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QM/PSK VOICE/DATA MODEM

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16. Abstract

Two Quadrature Modulation/Phase Shift Keyed (QM/PSK) Voice/Data Modem systems have been developed as part of the satellite communications hardware for advanced air traffic control systems. These systems consist of a modulator and demodulator unit which provides for the one-way communication of voice and/or data signals.

The modulator and demodulator unit provides simultaneous transmission of analog voice and digital data signals multiplexed on a single carrier, using quadrature modulation techniques. The modem interfaces with the transmitter/receiver at 70 MHz intermediate frequency.

The report contains design theory, circuit descriptions, diagrams, calibration procedures, and laboratory test results.

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PREFACE

The work presented in this final report was performed under contract and technical direction of the U.S. Department of Transportation, Transportation Systems Center. This hardware development was initiated as part of a DOT/FAA program to investigate satellite based air traffic control systems for oceanic aircraft. Testing and evaluation of advanced hardware and communications operations techniques was the specific application of the modem described herein.

The guidance and technical direction of Mr. Joseph Golab of TSC are hereby acknowledged.

METRIC CONVERSION FACTORS

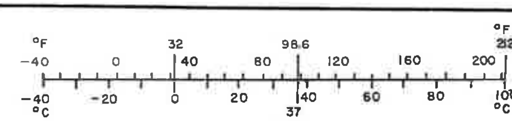
Approximate Conversions to Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
	LENGTH			
in	inches	*2.5	centimeters	cm
ft	feet	30	centimeters	cm
yd	yards	0.9	meters	m
mi	miles	1.6	kilometers	km
	AREA			
in^2	square inches	6.5	square centimeters	cm^2
ft^2	square feet	0.09	square meters	m^2
yd^2	square yards	0.8	square meters	m^2
mi^2	square miles	2.6	square kilometers	km^2
	acres	0.4	hectares	ha
	MASS (weight)			
oz	ounces	28	grams	g
lb	pounds	0.45	kilograms	kg
	short tons (2000 lb)	0.9	tonnes	t
	VOLUME			
tsp	teaspoons	5	milliliters	ml
Tbsp	tablespoons	15	milliliters	ml
fl oz	fluid ounces	30	milliliters	ml
c	cups	0.24	liters	l
pt	pints	0.47	liters	l
qt	quarts	0.95	liters	l
gal	gallons	3.8	liters	l
ft^3	cubic feet	0.03	cubic meters	m^3
yd^3	cubic yards	0.76	cubic meters	m^3
	TEMPERATURE (exact)			
°F	Fahrenheit temperature	5/9 (after subtracting 32)	Celsius temperature	°C

*1 in = 2.54 (exactly). For other exact conversions and more detailed tables, see NBS Misc. Publ. 286, Units of Weights and Measures, Price $2.25, SD Catalog No. C13.10:286.

Approximate Conversions from Metric Measures

Symbol	When You Know	Multiply by	To Find	Symbol
	LENGTH			
mm	millimeters	0.04	inches	in
cm	centimeters	0.4	inches	in
m	meters	3.3	feet	ft
m	meters	1.1	yards	yd
km	kilometers	0.6	miles	mi
	AREA			
cm^2	square centimeters	0.16	square inches	in^2
m^2	square meters	1.2	square yards	yd^2
km^2	square kilometers	0.4	square miles	mi^2
ha	hectares (10,000 m^2)	2.5	acres	
	MASS (weight)			
g	grams	0.035	ounces	oz
kg	kilograms	2.2	pounds	lb
t	tonnes (1000 kg)	1.1	short tons	
	VOLUME			
ml	milliliters	0.03	fluid ounces	fl oz
l	liters	2.1	pints	pt
l	liters	1.06	quarts	qt
l	liters	0.26	gallons	gal
m^3	cubic meters	35	cubic feet	ft^3
m^3	cubic meters	1.3	cubic yards	yd^3
	TEMPERATURE (exact)			
°C	Celsius temperature	9/5 (then add 32)	Fahrenheit temperature	°F



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ILLUSTRATIONS (CONT.)

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1. INTRODUCTION

Two Quadrature Modulation/Phase Shift Keyed Voice/Data Hybrid* Modem systems were delivered to the Department of Transportation under contract DOT-TSC-631. Each system consists of a Modulator and Demodulator unit, which provide for the one way communication of voice or data signals. The Hybrid Modem provides three modes of operation:

a. Voice only - Voice signals are Quadrature Modulated onto a 70 MHz carrier for transmission.

b. Data Only - 1200 BPS or 2400 BPS data signals are DCPSK modulated onto a 70 MHz carrier for transmission.

c. Voice plus Data - Voice and data signals are modulated onto the 0° and 90° phase components of the 70 MHz for transmission.

The modulation techniques employed in the Hybrid Modem will be tested over a ground to airborne satellite communication link. The Hybrid Modem will provide a test bed for demonstrating the feasibility of using Quadrature Voice Modulation techniques in future airborne satellite communication systems.

In the voice only mode the Quadrature Modulation technique is designed to provide intelligible voice communication down to C/N_o levels of 37 dB-Hz and lower. In the Voice plus Data mode the Hybrid Modem provides for simultaneous transmission of voice and data signals on a common carrier. The transmitted power

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*Hereafter, in this report, referred to as Hybrid Modem.

is split evenly between the 0° voice component and the 90° data component. Since Quad Mod is an analog voice system, the transmitted power is only shared between voice and data during periods of voice communication. Because of the periodic nature of voice communications, the large percentage of the transmitter power is devoted to the data signal. The voice signal is therefore transmitted simultaneously with the data but at little sacrifice to transmitted data power and system error rate performance. The Hybrid Modem System is a C.W. system for all three modes of operation, which allows its use in satellite networks where hard limiting receiver/transmitters are used.

1.1 General Description

A front view photograph of the Hybrid Modem Modulator and Demodulator units is shown in figure 1-1. At the Modulator front panel jacks are provided for the connection of external voice and data signals. Voice signals may be provided from a low impedance microphone (Z_o =150 ohms) or from a tape source at 600 ohms. A front panel audio gain control is provided for adjusting audio input levels to 0-V-U monitored at the panel V-U meter. The modulator accepts external data and clock signals at 1200 BPS or 2400 BPS. The Modulator also provides for the transmission of internally generated pseudo-noise binary sequences of 6,7 or 11 bits in length and at bit rates of 1200 BPS or 2400 BPS. The Modulator provides a 70 MHz carrier signal at 0 dBm (50 ohms) for connection to the transmitter.

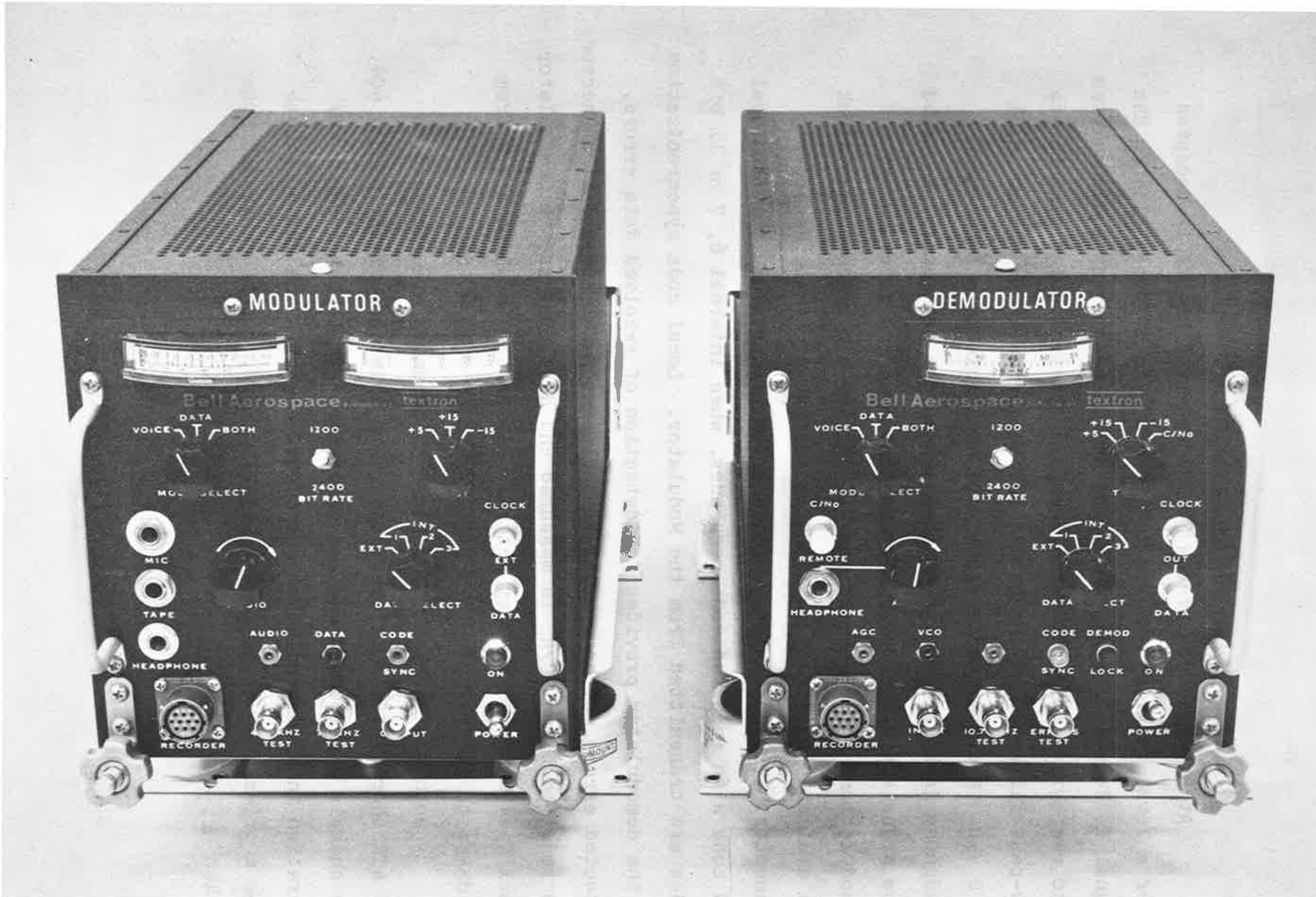


FIGURE 1-1. HYBRID MODEM #1 SYSTEM

At the Demodulator the 70 MHz received signal is accepted over a level range of -20 dBm to +10 dBm into 50 ohms. The 70 MHz signal is down-converted to 455 KHz and then coherently demodulated into respective voice or data signals. Received voice signals are low-pass filtered, de-emphasized and amplified to an output level of 0 V-U. Received audio signal are available at a front panel headphone jack or at the front panel Recorder connector. Received data signals are optimally filtered and detected after coherent demodulation. The detected data signal and bit synchronized clock are available at front panel BNC connectors or at the Recorder connector. The demodulator provides for synchronization of a local P/N code with received code sequences, when internal 6, 7 or 11 bit codes are transmitted from the Modulator. Local code synchronization at the demodulator provides for detection of received data errors. Detected errors may be counted at the front panel Error Test connector. The received signal C/N_o is measured and displayed at the demodulator panel Test meter. The Test meter is calibrated in dB-Hz steps from 35 dB-Hz to 55 dB-Hz.

Both the Modulator and Demodulator units are packaged in 3/4 ATR short chassis in accordance with ARINC Specification No. 404. The chassis are mounted on shock and vibration isolated racks for operation in a commercial airborne environment. The units operate from a primary power source of 115 VAC ± 10%, single phase and 50Hz to 440 Hz.

1.2 Quadrature Modulation Techniques

The block diagram in Figure 1-2 illustrates the operation of the quadrature voice modulator. The preprocessed voice signal, V (t), is fed to a balanced modulator together with a signal, $\sin w_o t$. (The preprocessing, which consists of high frequency pre-emphasis and amplitude limiting, will be discussed later.) The output of the modulator is the product of V(t) and $\sin w_o t$, which is a suppressed carrier amplitude modulated signal. The signal $\sin w_o t$ is also phase shifted by 90° to yield $\cos w_o t$, which is added to $V(t) \sin w_o t$. The output of the adder is $V(t) \sin w_o t + \cos w_o t$. The vector diagram in Figure 1-3 shows the various signals which occur in the modulator. Up to this point the circuitry is similar to an Armstrong FM modulator, except the preprocessing is different and the amplitude ratio of $V(t) \sin w_o t$ to $\cos w_o t$ is large as compared with an Armstrong FM modulator. In an Armstrong modulator the amplitude ratio of $V(t) \sin w_o t$ to $\cos w_o t$ is kept small so that the sum signal $V(t) \sin w_o t + \cos w_o t$ is essentially a constant envelope signal; and the sum signal is fed to a high ratio frequency multiplier to yield a high deviation FM or PM signal. In the quadrature modulator the sum signal $V(t) \sin w_o t + \cos w_o t$ is not a constant envelope signal because $V(t) \sin w_o t$ can be larger than $\cos w_o t$. To yield a constant amplitude signal, the sum signal is passed through a hard limiter as shown in Figure 1-2. The quadrature modulator generates a constant envelope carrier of frequency $w_o/2\pi$ and phase angle $\rho(t)$, where $\rho(t) = \tan^{-1} V(t)$. This constant envelope carrier can now be readily transmitted using efficient Class-C amplifiers.

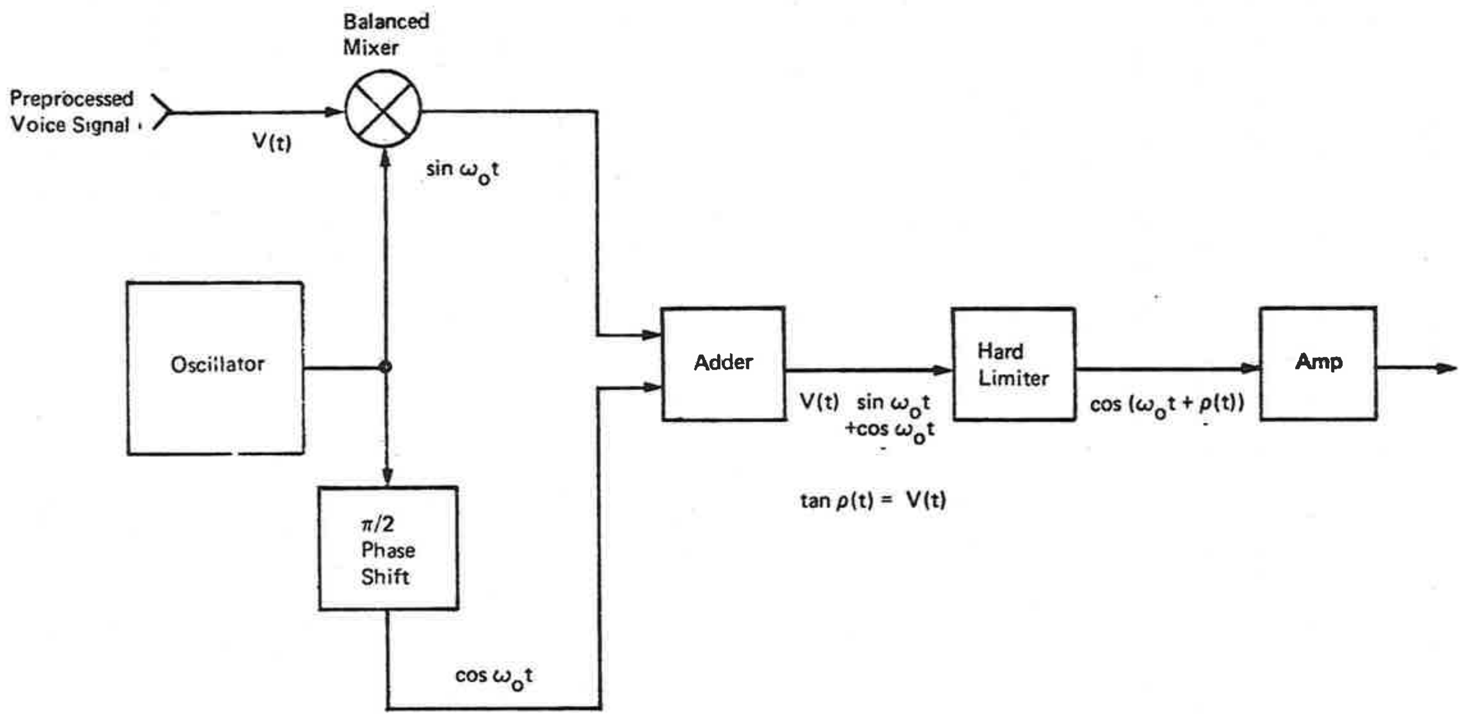


FIGURE 1-2. QUADRATURE MODULATION BLOCK DIAGRAM (VOICE MODE)

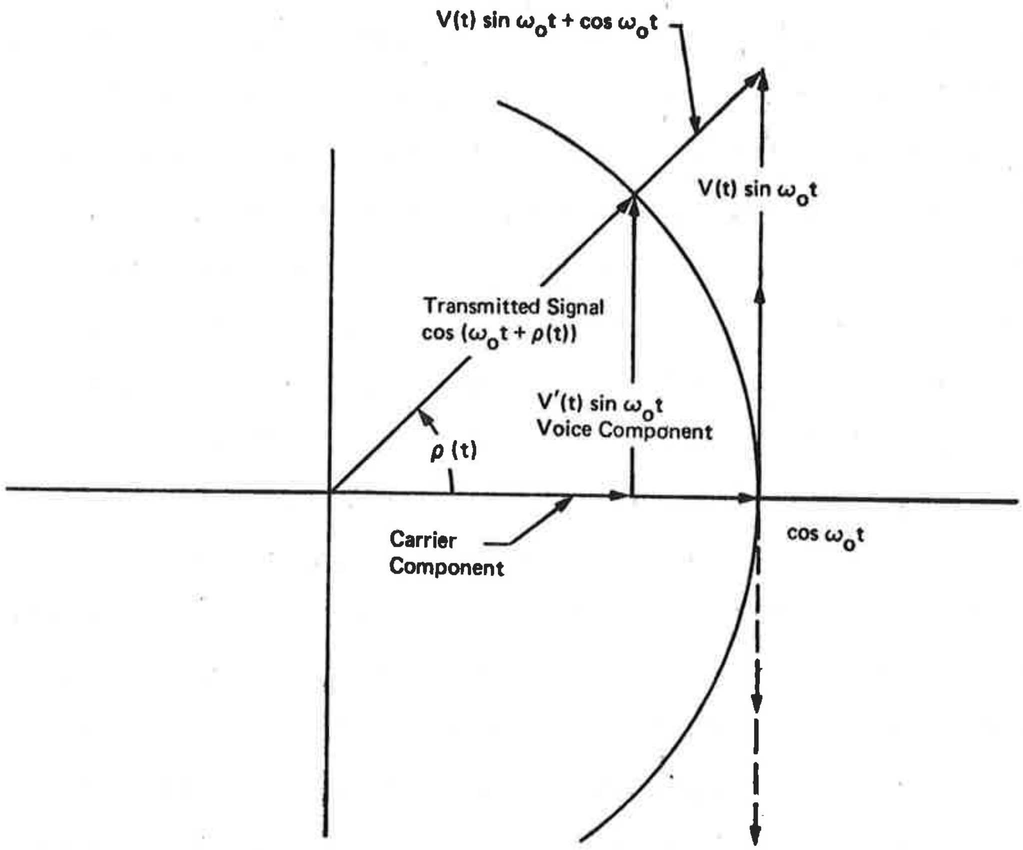


FIGURE 1-3. QUADRATURE MODULATION VECTOR DIAGRAM

The angle of voice modulation, $\rho(t)$, determines the ratio of power in the carrier, cos $w_o t$, to the power in the voice component, $V(t)$ sin $w_o t$. If the maximum angle of modulation is held to $\rho_{max}(t) = 72°$ then at peak voice modulation 10% of the total transmitter power is in the carrier and 90% of the power is in the voice signal. At the demodulator, for a total received signal-to-noise spectral density (C/N_o) of 46 dB-Hz, for example, the minimum carrier C/N_o would be 36 dB-Hz and the voice C/N_o would be 45.5 dB-Hz at periods of peak modulation. A more realistic indication of the respective carrier power versus voice sideband power is based on the RMS angle of modulation ρ_{rms}. Prior to Quadrature Modulation the voice signal is processed through a pre-emphasis network, 20 dB compressor and 300 Hz to 3500 post filter. Test results have shown that the degree of repeaking after post filtering of a clipped voice signal is about 4.0 dB. The respective peak to RMS ratio of the preprocessed voice signal at the Quadrature Modulator is 4.0 dB. For peak modulation angles of 72° the RMS modulation angle is about 45°. Under normal periods of voice reception the average power in the received carrier is equal to the power in the voice side-band. An even distribution of power in the carrier and voice sidebands provides for adequate carrier tracking at the coherent demodulator. Momentary drops in carrier power at peak modulation angles, have no effect on the carrier tracking performance of the coherent demodulator.

The block diagram in Figure 1-4 illustrates the operation of the quadrature voice modulator in combination with the transmission of Differentially Coherent Phase Shift Keyed Data (DCPSK). The pre-processed voice signal is balanced modulated onto the sin $w_o t$, in-phase carrier component. The cos $w_o t$ quadrature component is now fed to a Phase Shift Key (PSK) modulator where the cos $w_o t$ carrier is modulated with differentially encoded data. The voice and data signals are added together and then passed through a hard limiter. The vector diagram in Figure 1-5 shows the various signals as they appear in the modulator. Referring to Figure 1-5, the voice signal maintains the correct polarity, as either a binary "0" (cos $w_o t$) or a binary "1" (cos $w_o t$ + 180°) is transmitted. The amplitude of the voice vector V (t) sin $w_o t$ is dependent only on the angle of modulation, ρ (t). The data carrier, cos ($w_o t$ + (nT)), maintains the correct phase of 0° or 180° regardless of the voice signal level. The amplitude of the data vector is amplitude modulated by the voice signal. During periods of voice transmission, power is diverted from the data carrier and placed in the voice carrier. The angle of modulation, ρ (t), determines the ratio of data power to voice power. Selection of $\rho_{max}(t)$ will depend on system requirements, such as required received voice intelligibility, data bit rate and received data bit error rate. For the present Advanced Modem system, the angle of modulation is chosen such that the transmitter power is split evenly between the voice and data signal during periods of voice transmission. The peak modulation angle, ρ_{max} (t), is set at 58°. As stated previously, the peak-to-RMS ratio of the preprocessed audio signal is 4 dB and the resulting RMS modulation angle is 37°.

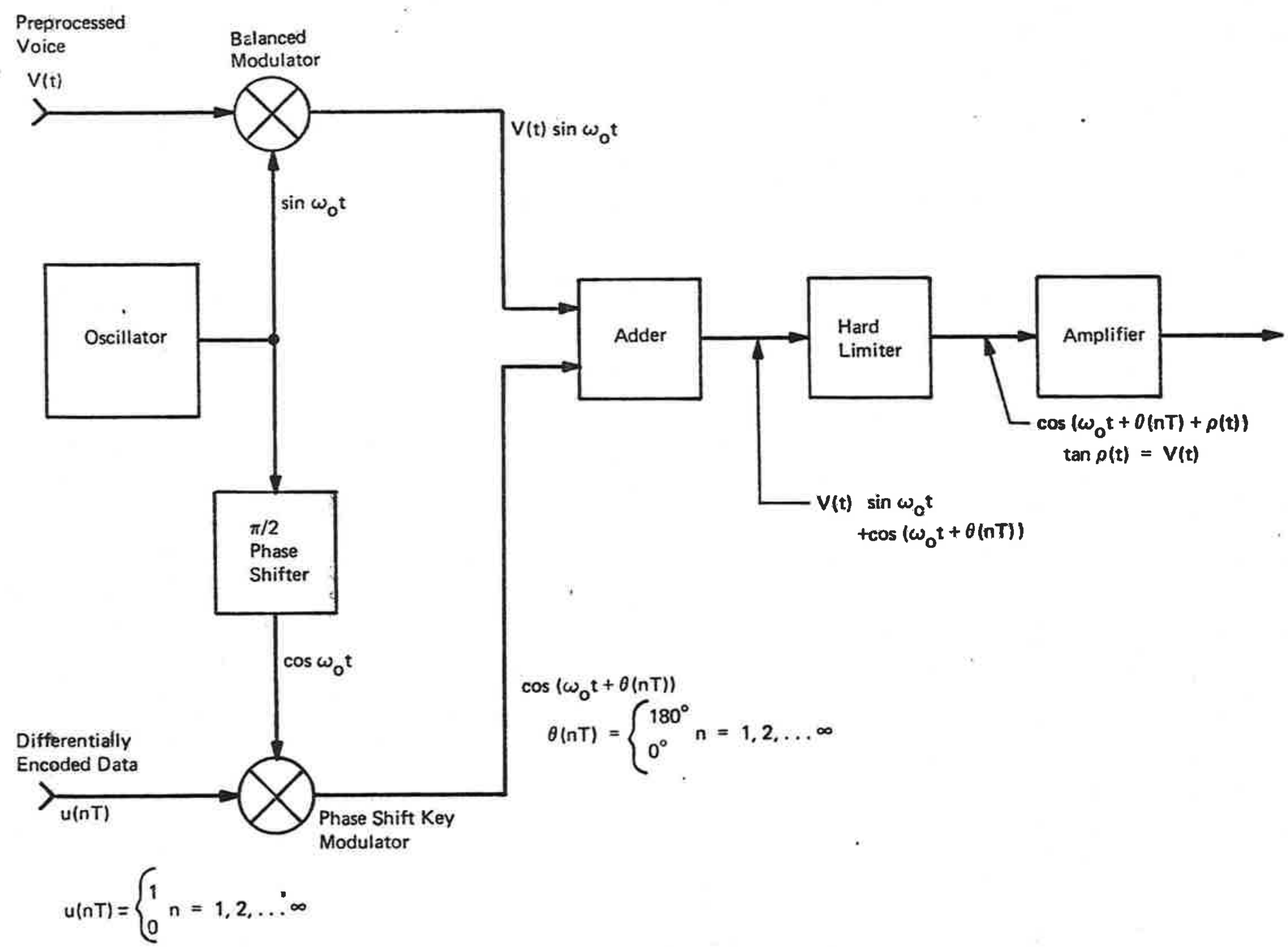


FIGURE 1-4. QUADRATURE MODULATION BLOCK DIAGRAM (VOICE PLUS DATA MODE)

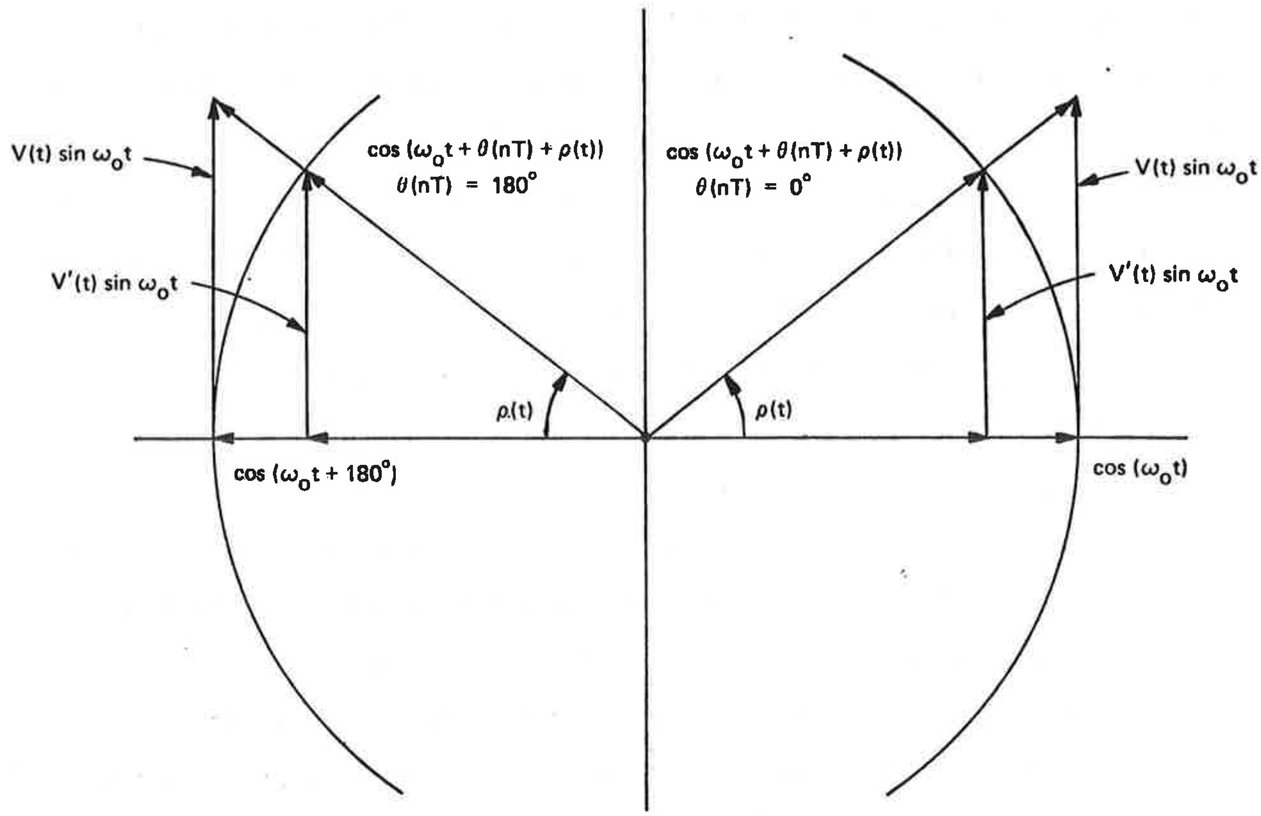


FIGURE 1-5. QUADRATURE MODULATION VECTOR DIAGRAM (VOICE PLUS DATA MODE)

2. SYSTEM DESIGN

2.1 Modulator

A block diagram of the Hybrid Modem Modulator is shown in figure 2-1 and a detailed wiring diagram of the Modulator is shown in figure 5-1. The Modulator consists of two audio boards, A2 and A13, which accept audio signals from a microphone or tape recorder source. All audio signals are processed through a pre-emphasis and voltage compressor network prior to modulation. Two digital data boards, A4 and A6, provide for the transmission of 1200 BPS or 2400 BPS data. This data may be internally generated pseudo noise codes or external data. All data signals are differentially encoded prior to modulation. The Quadrature Modulator board, A11, provides for the modulation of all voice and data signals onto a 455 KHz carrier. The 455 KHz modulated carrier is connected to the R.F. Up-Converter Module, A15, where the signal is converted to a final output carrier frequency of 70 MHz.

2.1.1 Voice Processing

A block diagram of the Audio Input Network and Voice Processor is shown in figure 2-2. Detailed schematic diagrams of boards A2 and A13 are shown respectively in figures 5-2 and 5-3.

The voice signal is processed at the Modulator to provide maximum received signal-to-noise ratio for the voice signal at the demodulator. In figure 2-2 the voice signal is passed through a 1:1 transformer to a high pass R-C network at the input to amplifier A1. The input transformer and high pass R-C network are designed to

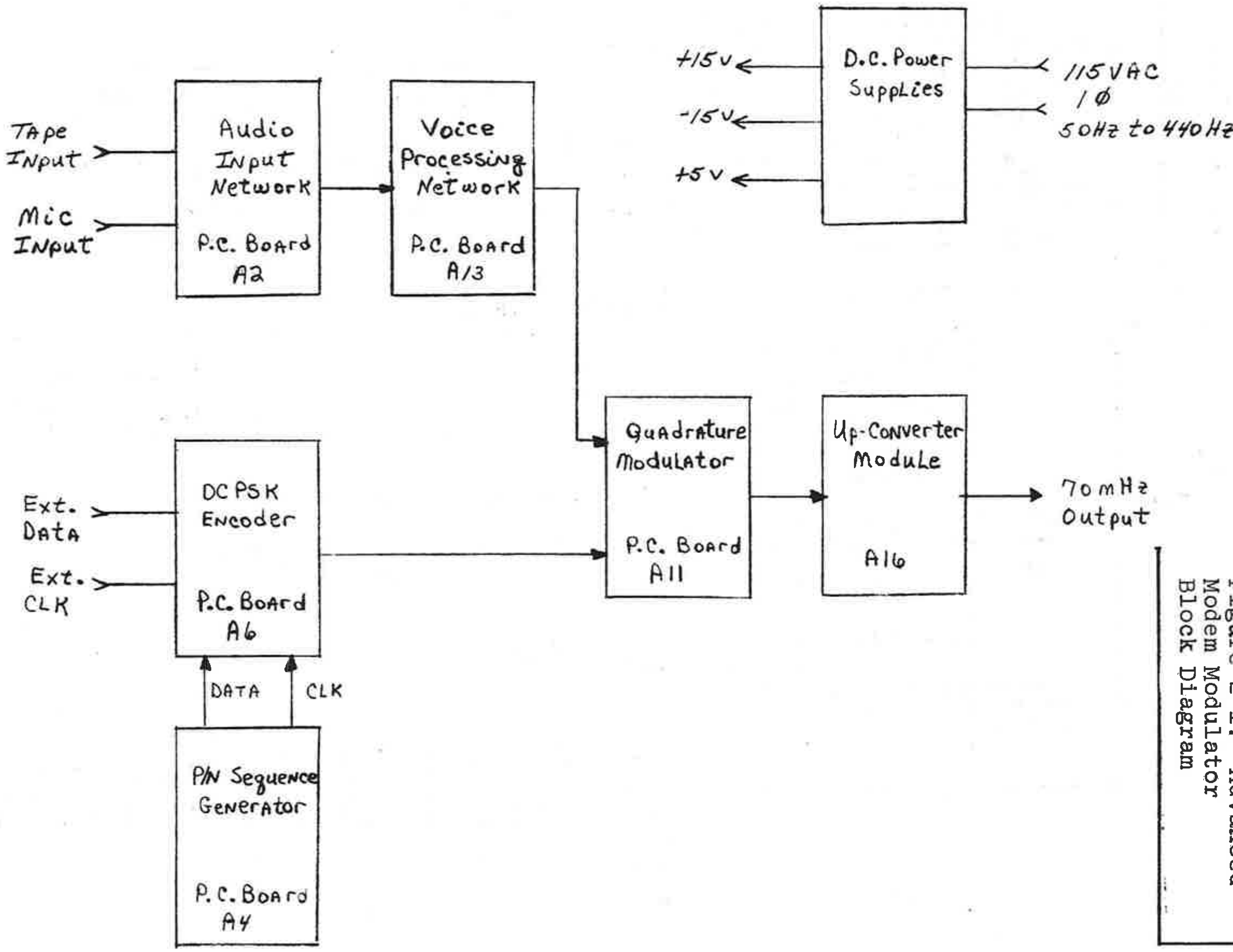
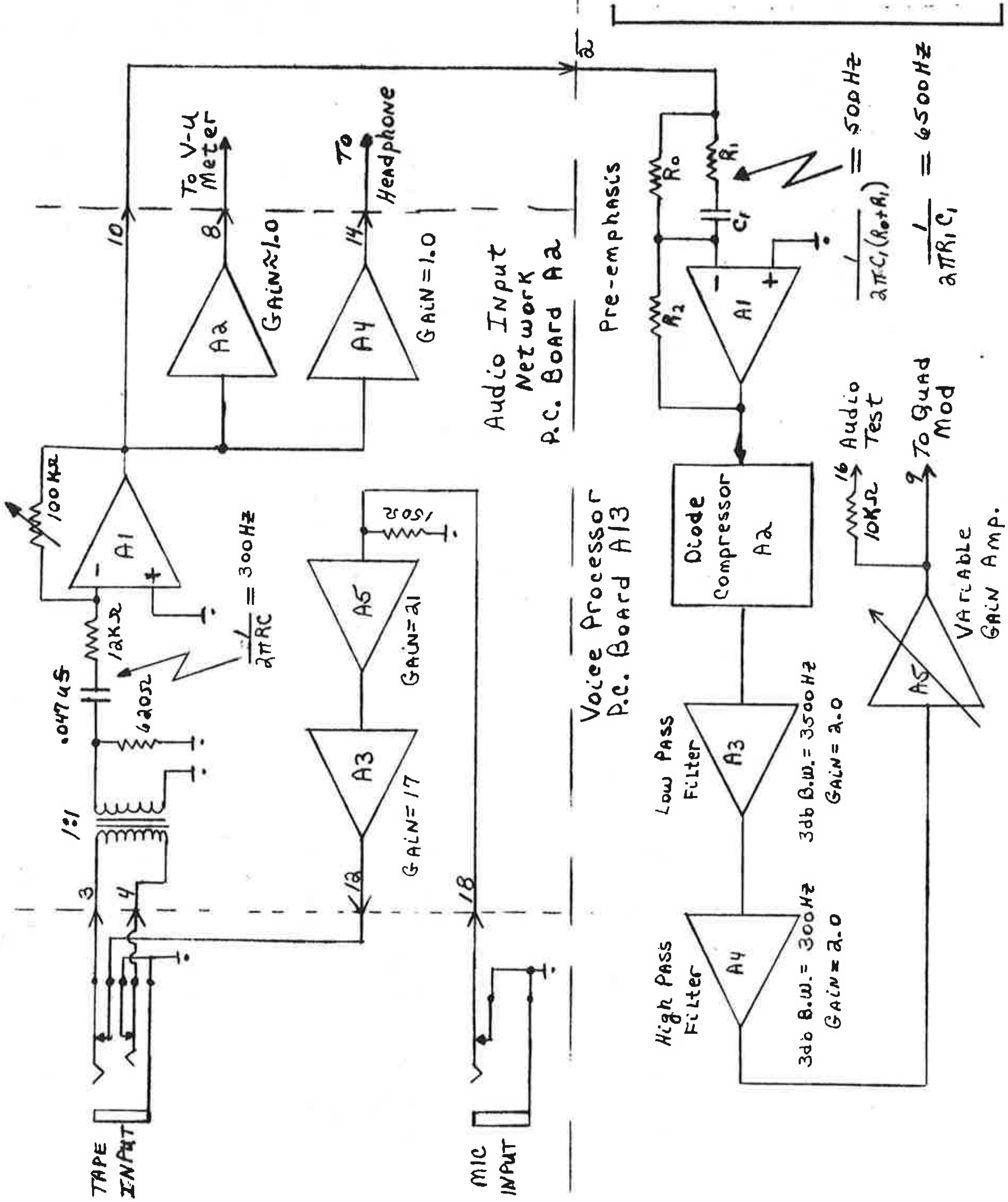


Figure 2-1: Advanced Modem Modulator Block Diagram

Figure 2-2: Voice Processor Block Diagram



attenuate all low frequency voice components below 300 Hz. Voice frequency components below 300 Hz contribute little to the overall speaker intelligibility, and transmitter power should be conserved for the transmission of voice signals which contribute most to received voice intelligibility. Secondly, it is desired to eliminate voice signals which are low in frequency and within the noise bandwidth of the carrier tracking loop of the coherent demodulator. At the receiver the 6 dB bandwidth of the carrier tracking loop is 150 Hz. Any voice components within this loop bandwidth tend to disrupt the demodulator carrier tracking performance. The frequency response of the audio input network at board A2 is plotted in figure 2-3. It is seen that frequencies below 100 Hz are severely attenuated. The received audio signal is amplified by A1, as shown in figure 2-2, and supplied as an input signal to the Voice Processor board. Amplifier A1 on board A2 is a variable gain amplifier whose gain is controlled by the front panel AUDIO gain control. The audio level at the output of A1 is monitored at the panel V-U meter. The AUDIO gain control should be set for peak readings of 0 V-U at the meter.

The voice signal from board A2 is fed to pre-emphasis network, A1, on board A13. The pre-emphasis network provides +6 dB/octave increase in AC gain from 500 Hz to 6500 Hz. The typical voice spectrum is not flat over frequency, and high frequency voice components are often masked by noise in many communication systems. The pre-emphasis network is designed to equalize the voice spectrum over the entire frequency range. The frequency response of the pre-emphasis

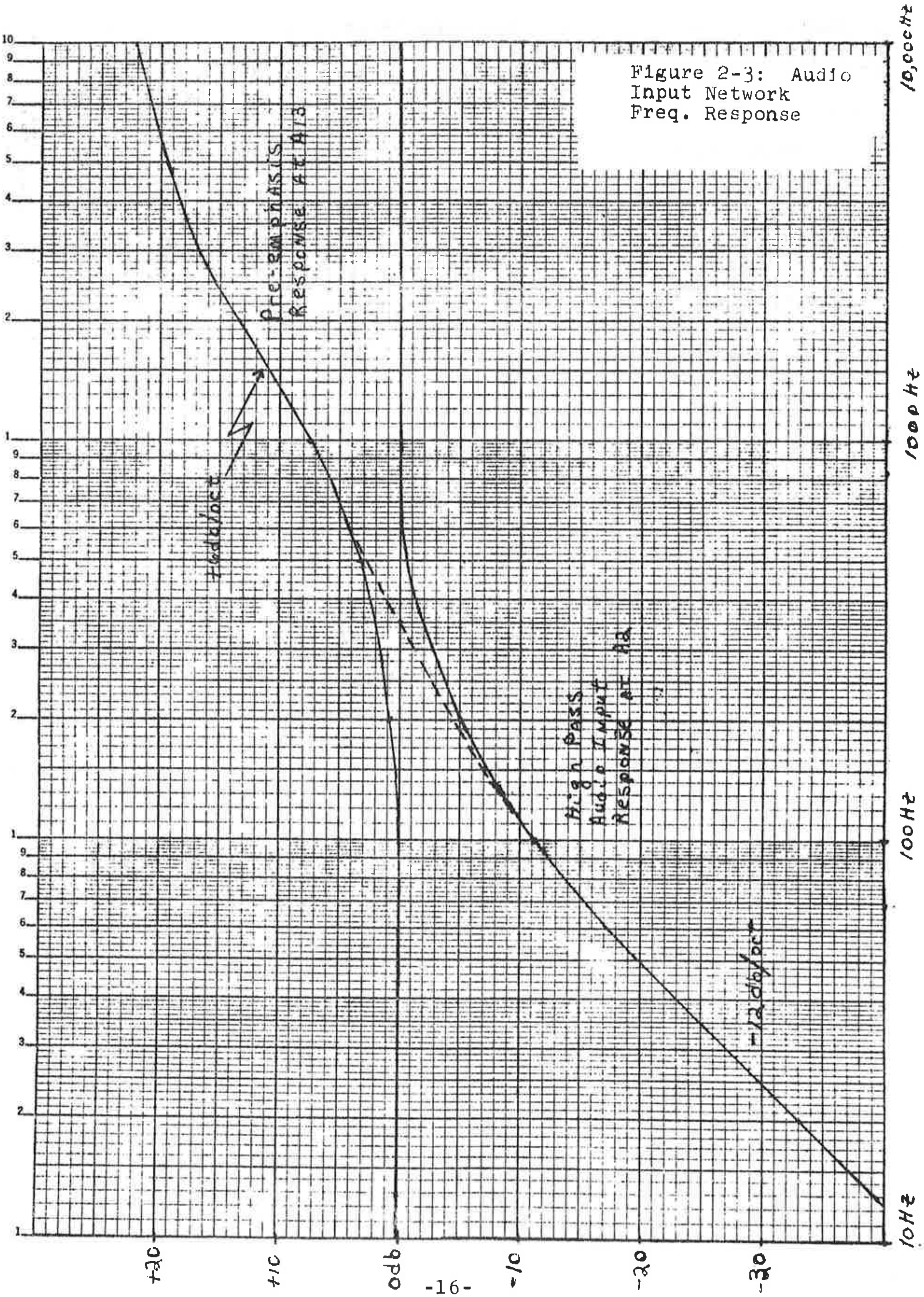


Figure 2-3: Audio Input Network Freq. Response

network is plotted in figure 2-3. The composite response of the Audio Input board and the pre-emphasis amplifier is shown in figure 2-3. It is clear in figure 2-3 that low frequency voice components which contribute little to voice intelligibility are attenuated, while higher frequency components are amplified to equalize the overall voice spectrum.

Frequency processing is one part of equalizing the voice signal. Not only is the voice spectrum unbalanced with respect to frequency, but the amplitude distribution of the voice signal varies greatly. The peak to RMS ratio for typical speakers often reaches 20 dB. Very little information is carried in the random peaks of a speaker, and communication systems which try to linearly transmit and receive voice signals often suffer serious degradation under low SNR conditions. To increase the level of the lower power voice components, the audio signal is often processed through a clipper. A clipper will chop off high level voice peaks and will linearly pass the low level voice signals. A clipper will introduce distortion in the voice signal, which often results in a deterioration in speaker intelligibility at clipping levels greater than 24 dB. To reduce the harmonic distortion of a clipper, a compressor is often used to reduce the peak to RMS ratio of a voice signal. As shown in figure 2-2, the voice signal from the pre-emphasis network is connected to a diode voice compressor. The voltage transfer characteristic of the compressor is shown in figure 2-4. The compressor has a gain of 26 dB for low level input signals and unity gain for high level signals. Large voice peaks are rounded off rather than clipped,

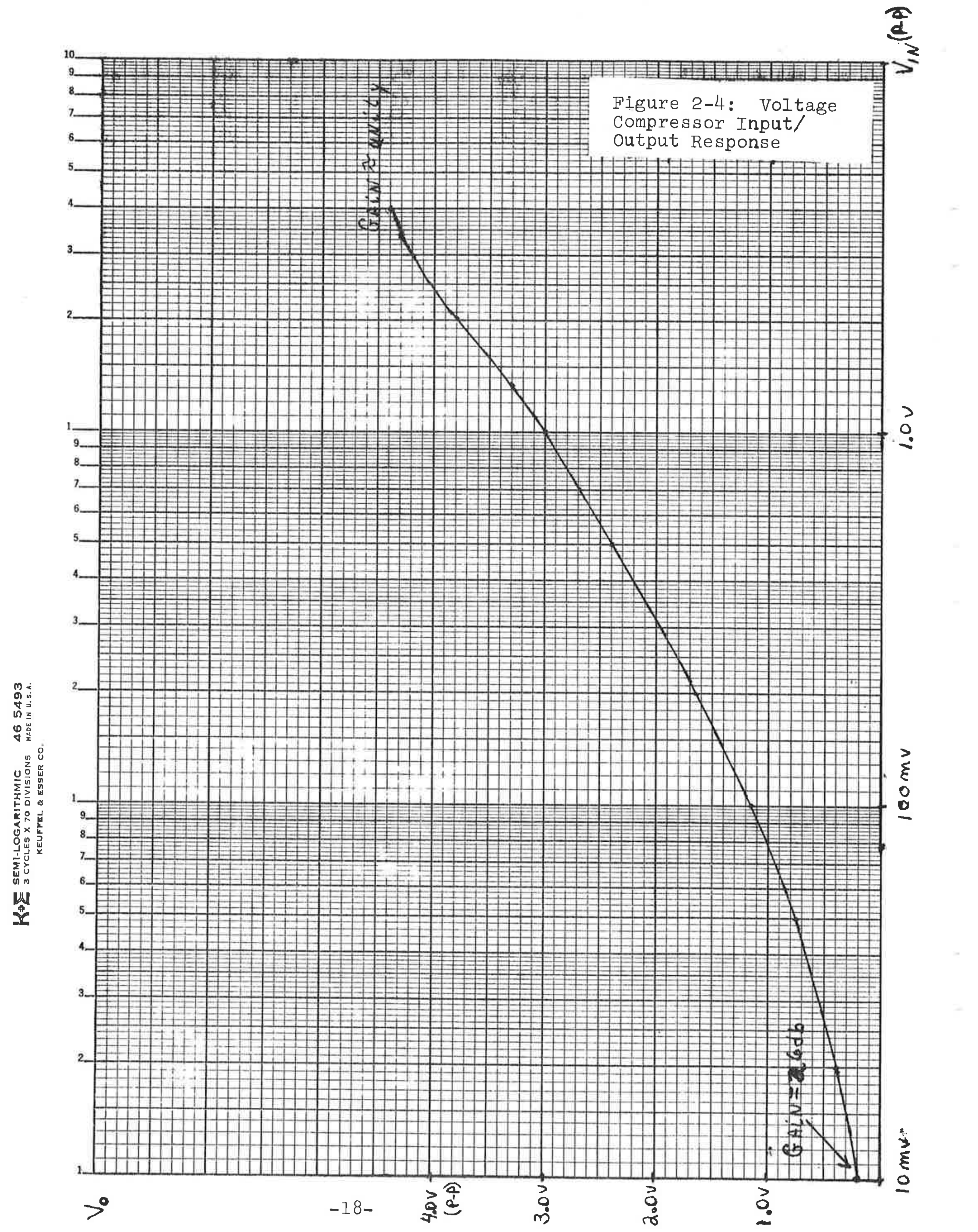


Figure 2-4: Voltage Compressor Input/ Output Response

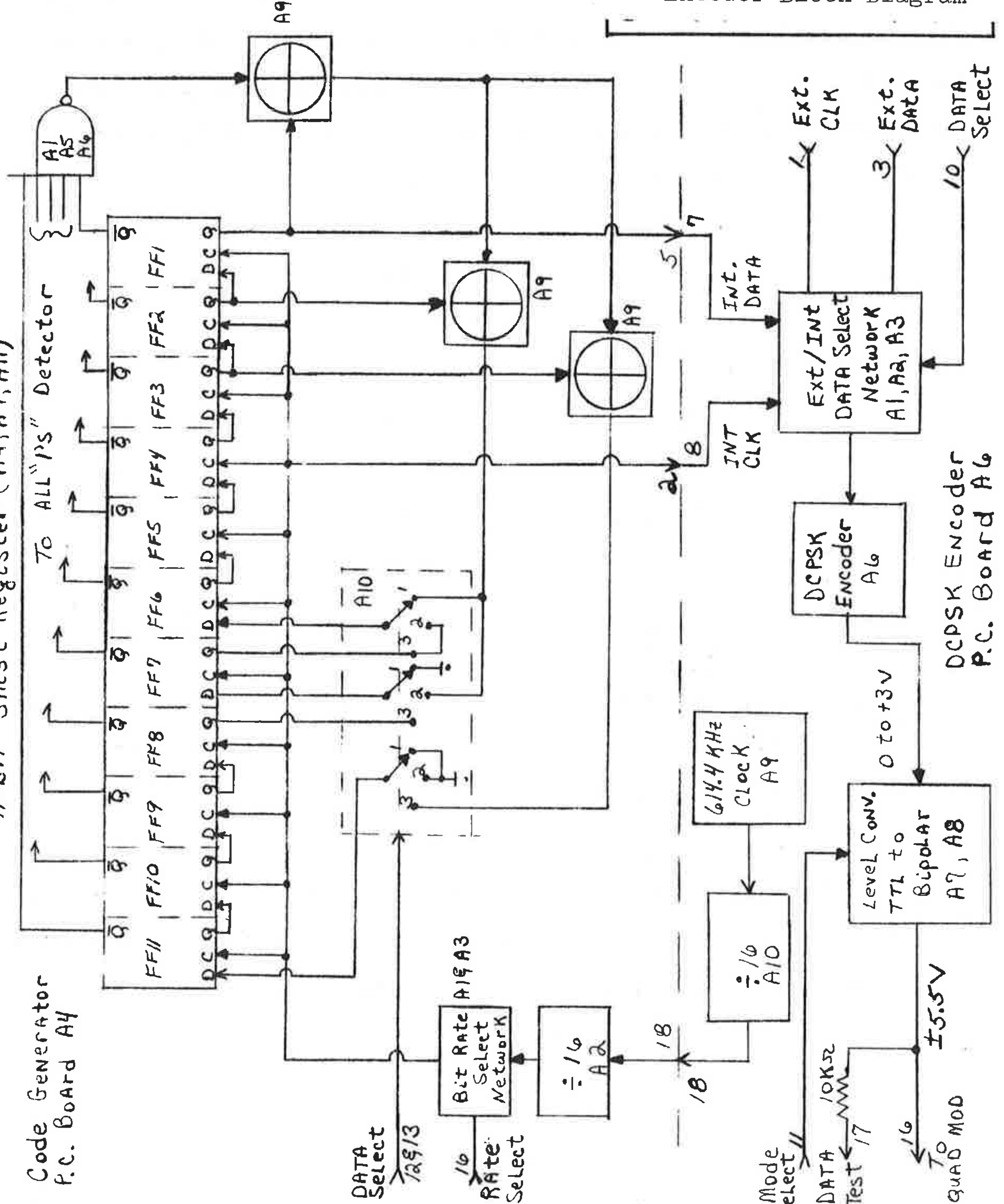
thus reducing the harmonic distortion common to a clipper. The peak to RMS ratio of the Voice signal is reduced by the compressor, such that the low level phonemes of a speaker are now higher in power. It is the low level phonemes of a voice signal which determine speech intelligibility. When these signals are masked by noise, speech intelligibility is reduced. The compressor amplifies low level phonemes and reduces random peak signals, thus normalizing the amplitude distribution of the voice signal.

The processed voice signal is passed through a set of low pass and high pass filters prior to modulation. In figure 2-2, a 3500 Hz, 2 pole, low pass butterworth filter is used to restrict the transmission bandwidth and remove unwanted harmonic signals outside the band of interest. A 300 Hz 2-pole high pass butterworth filter provides additional filtering of undesired low frequency voice components that are amplified by the compressor. The post filtering of the compressed signal introduces some repeaking of the voice signal, about 4 dB. The signal from high pass filter A4 is fed to a variable gain amplifier, A5, which controls the level of audio modulation at the Quadrature Modulator. The level output of A5 is set to ±9 volts for nominal input levels of 0 V-U as monitored at the front panel V-U meter.

2.1.2 <u>Data Code Generator</u>

A block diagram of the Data Code Generator and DCPSK Encoder Network is shown in figure 2-5 and detailed schematic diagrams of boards A2 and A4 are shown respectively in figures 5-4 and 5-5.

Figure 2-5: Data Code Generator & DCPSK Encoder Block Diagram



The Hybrid Modem Modulator is designed to transmit digital data at bit rates of 1200 BPS or 2400 BPS. This data may be either external or internal as selected at the front panel DATA SELECT switch. External data and clock signals may be connected to front panel BNC connectors of the Modulator. The Modulator also provides for the transmission of three separate pseudo noise codes, as selected by DATA SELECT switch. In the block diagram of figure 2-5 an eleven bit shift register is used to generate any of three P/N sequences. The characteristics of the three P/N codes are listed as follows:

Switch Position	Code Length		Code Polynomial
INT1	6 bits	2^6-1	x^6+x+1
INT2	7 bits	2^7-1	x^7+x+1
INT3	11 bits	$2^{11}-1$	$x^{11}+x^2+1$

The selected code sequence and clock signal is fed to the Differential Encoder network at P.C. board A6. The digital data is differentially encoded as follows:

INPUT BIT AT T=N	TRANSMITTED BIT AT T=N-1	TRANSMITTED BIT AT T=N
0	0	0
0	1	1
1	0	1
1	1	0

The sequence of encoded data is converted from a TTL compatible signal to a bipolar analog signal at the level converter network on P.C. board A6. The bipolar data signal is then connected to the Quadrature Modulator. In the Data Mode and Data plus Voice Mode the amplitude of the data signal is ± 5.5V (Peak). In the Voice Mode the output of the level converter network is a constant -2.6 VDC. The D.C. level from the DCPSK Encoder in the Voice Mode is used to continuously modulate the residual carrier component of the voice signal.

2.1.3 Quadrature Modulator

A block diagram of the Quadrature Modulator is shown in figure 2-6 and a detailed schematic diagram of P.C. board A11 is shown in figure 5-6. At the Quadrature Modulator, the audio and data signals are modulated onto the 0° and 90° phase components of a 455 KHz carrier. The 455 KHz carriers at 0° and 90° are generated in a digital quadrature hybrid, which divides a 1.82 MHz reference frequency by a factor of four. A timing diagram of the division sequence is shown in figure 2-6. A digital quad hybrid configuration was chosen to generate the reference carriers, because a high degree of quadrature balance is required to eliminate channel cross-talk. Conventional passive quadrature hybrids only guarantee a quadrature accuracy of 90° ± 1°. The digital hybrid used on board A11 is built with Schottky TTL logic circuits. The variation in delay through the N74S113 J-K flip-flops is 5 nsec ±2 nsec. At 455 KHz 2 nsec represents a phase error of only 0.33°. For a quadrature error of 0.33° the level of data at the audio channel is down 45 dB. The quadrature carriers are fed through level translators to double balanced mixers. The modulated carriers are summed together in wideband amplifier A2 and then fed through bandpass limiter A1. A nearly constant amplitude

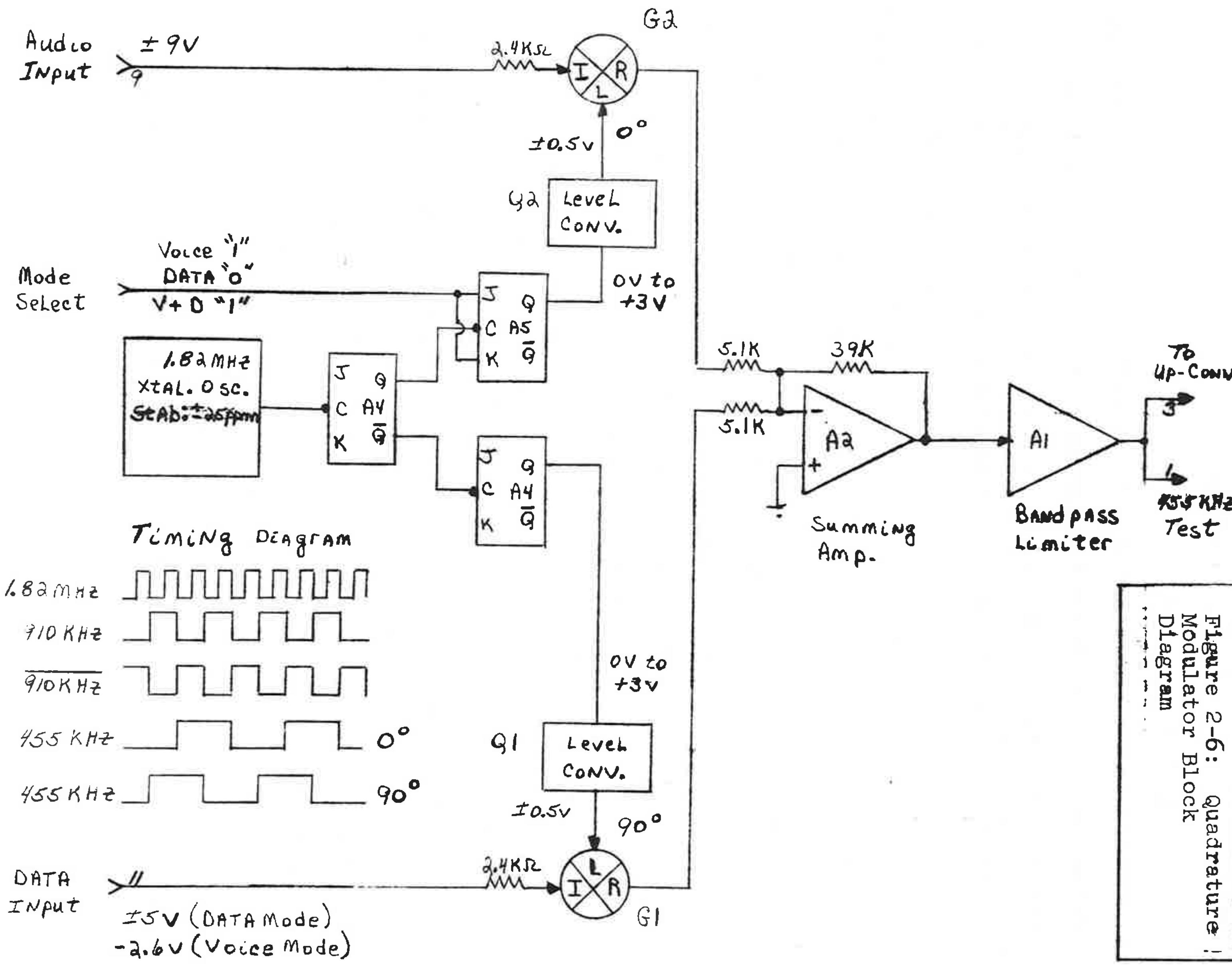


Figure 2-6: Quadrature Modulator Block Diagram

signal at 455 KHz is fed to the Up-Converter module. Further limiting of the Quad ModeSignal in the Up-Conversion process quarantees a C.W. signal at 70 MHz.

2.1.4 Up-Converter Module

A block diagram of the Up-Converter Module is shown in figure 2-7 and a detailed schematic diagram of module A15 is shown in figure 5-7 The 455 KHz signal from the Quadrature Modulator is up-converted to 70 MHz in two conversion steps by module A15. An intermediate conversion frequency of 10.7 MHz is used at the up-converter because of the availability of standard I.F. filter components at this frequency. In figure 2-7 the 455 KHz signal is mixed with a 10.245 MHz L.O. signal to generate an upper sideband I.F. signal at 10.7 MHz. The 10.245 MHz L.O. signal is generated by a digital clock oscillator, whose temperature stability is ±25 ppm over 0°C to 50°C. The TTL compatible square wave from Y2 is filtered and amplified by A2 which is used as a driver amplifier to mixer G1. The upper and lower sideband output of G1 is fed to ceramic filter Y1, whose 3 dB band-width is 210 KHz and whose 40 dB bandwidth is 600 KHz. The ceramic filter providesaat least 50 dB suppression of the lower sideband signal at 9.790 MHz. The desired 10.7 MHz I.F. signal is further amplified by A1 and spplied to mixer G2. The L.O. frequency at G2 is generated from a 59.3 MHz crystal oscillator, whose temperature stability is ± 10 ppm over 0°C to 50°C. The upper sideband output from mixer G2 at 70 MHz is filtered and amplified by A3. Amplifier A3 is a double-tuned RF amplifier with tuned input and output stages. The output network of A3 is a 10 turn to 1 turn matching transformer, with

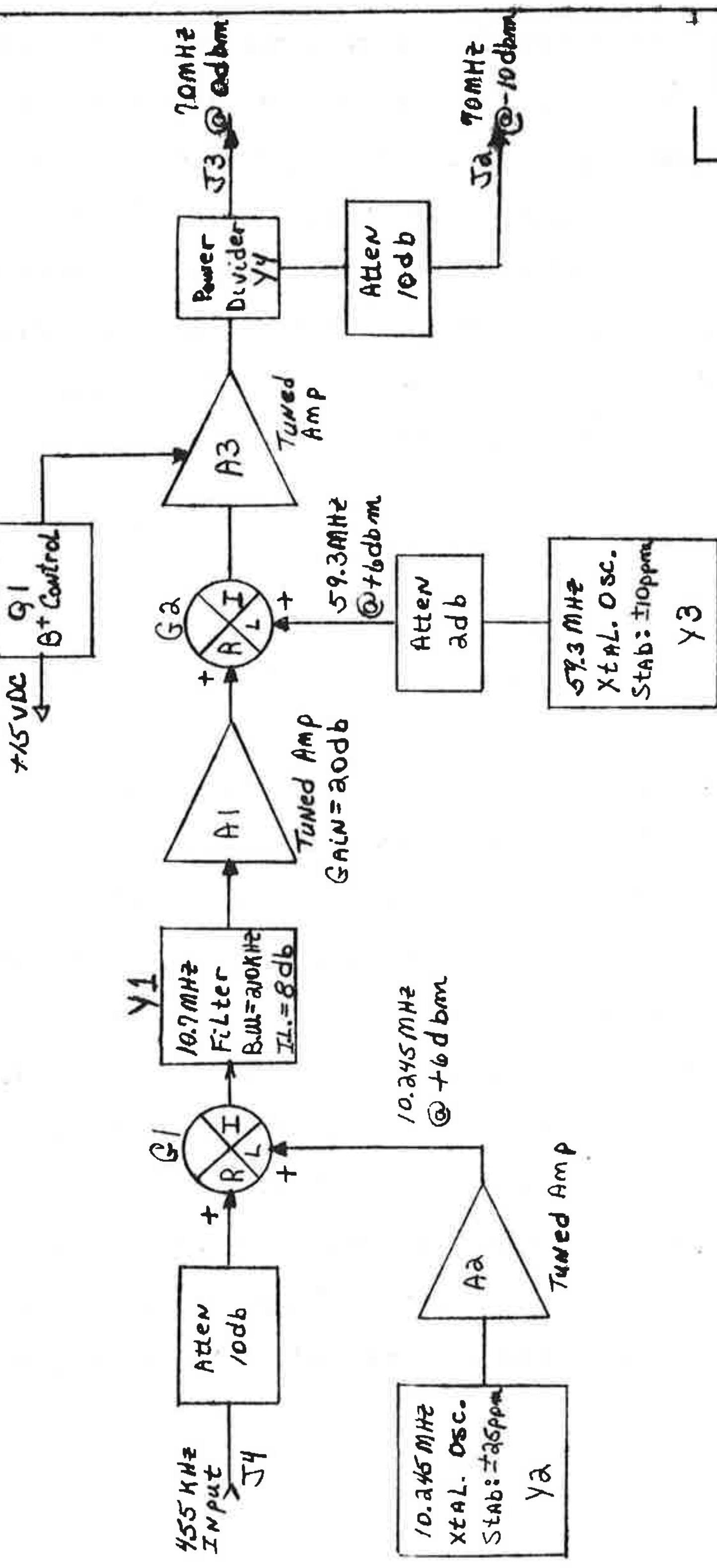


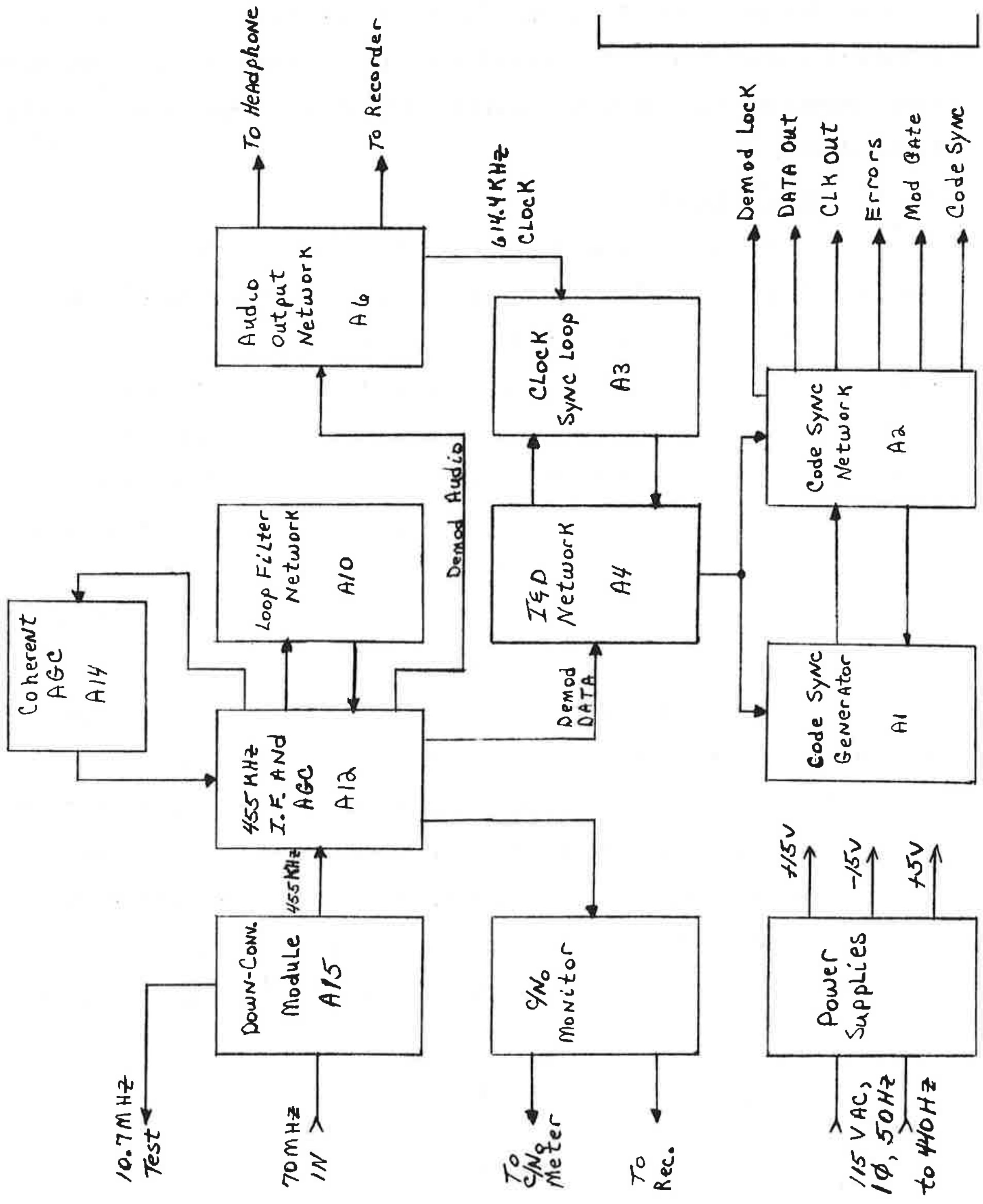
Figure 2-7: Up-Converter Block Diagram

a powdered iron turning core. The output level of A3 is controlled by adjusting the B+ voltage to the amplifier. The output power at the front panel 70 MHz OUTPUT connector is set at 0 dBm into a 50 ohm load. Amplifier A3 has a 3 dB bandwidth of 2 MHz and a 40 dB bandwidth 40 MHz. All spurious signals at the L.O. (59.3 MHz) and LSB (48.6 MHz) frequencies are suppressed at least 40 dB at the 70 MHz OUTPUT connector. The frequency stability of the 70 MHz signal is determined by the overall stability of the 1.82 MHz, 10.245 MHz and 59.3 MHz crystal oscillators which are used to generate the 70 MHz signal. The worst case drift in carrier frequency versus temperature (0°C to 50°C) is calculated to be + 860 Hz.

2.2 Demodulator

A block diagram of the Hybrid Modem Demodulator is shown in figure 2-8 and a detailed wiring diagram of the unit is shown in figure 5-8. The 70 MHz received signal plus noise is fed to the down-converter which translates the signal plus noise to 455 KHz. The 455 KHz IF & AGC Network, A12, and Loop Filter Network, A10, provide for the coherent demodulation of the received signal. The coherent demodulator operates in three modes: voice only, data only and voice plus data. The demodulated voice or data signals are fed to respective voice and data processing networks. A Coherent AGC Network, A14, is used to control a constant signal level at the input to the coherent demodulator. The demodulated audio signal is fed to the Audio Output Network, A6, where the voice signal is low pass filtered, de-emphasized and amplified to normal operating levels. The demodulated data is fed to the Integrate and Dump Network, A4, which

Figure 2-8: Demodulator Block Diagram



optimally filters and detects the received digital data. The detected data may be synchronized with local P/N Code Generators, A1, for the purpose of error detection. A C/N_0 Monitor Network, A8, is also designed into the Demodulator for the purpose of measuring received signal C/N_0. The signal C/N_0 is displayed on the Demodulator front panel meter, which is calibrated in dB-Hz steps from 35 dB-Hz to 55 dB-Hz.

2.2.1 Down-Converter

A block diagram of the Down-Converter is shown in figure 2-9 and a detailed schematic drawing of module A15 is shown in figure 5-9. Two stages of frequency conversion are used in translation of the 70 MHz signal to 455 KHz. I. F. frequencies at 10.7 MHz and 455 KHz are selected because of the availability of components at these standard I.F. frequencies. The Down-Converter accepts a 70 MHz signal plus noise over an input power range of -20 dBm to +10 dBm. A 20 dB attenuator is inserted at the input of amplifier A1 to protect the front end of A1 from limiting on high level input signals. Amplifier A1 is an MC1590G integrated circuit RF amplifier, built by Motorola. Tuned input and output L-C networks are used to match the amplifier to 50 ohms. The output of A1 is a 10 turn to 1 turn transformer with a powdered iron tuning slug. Amplifier A1 is designed to provide at least 40 dB of image frequency rejection at 48.6 MHz. Amplifier A1 also operates as an AGC amplifier. The gain of A1 is controlled by detecting the signal plus noise at 10.7 MHz and feeding back an AGC

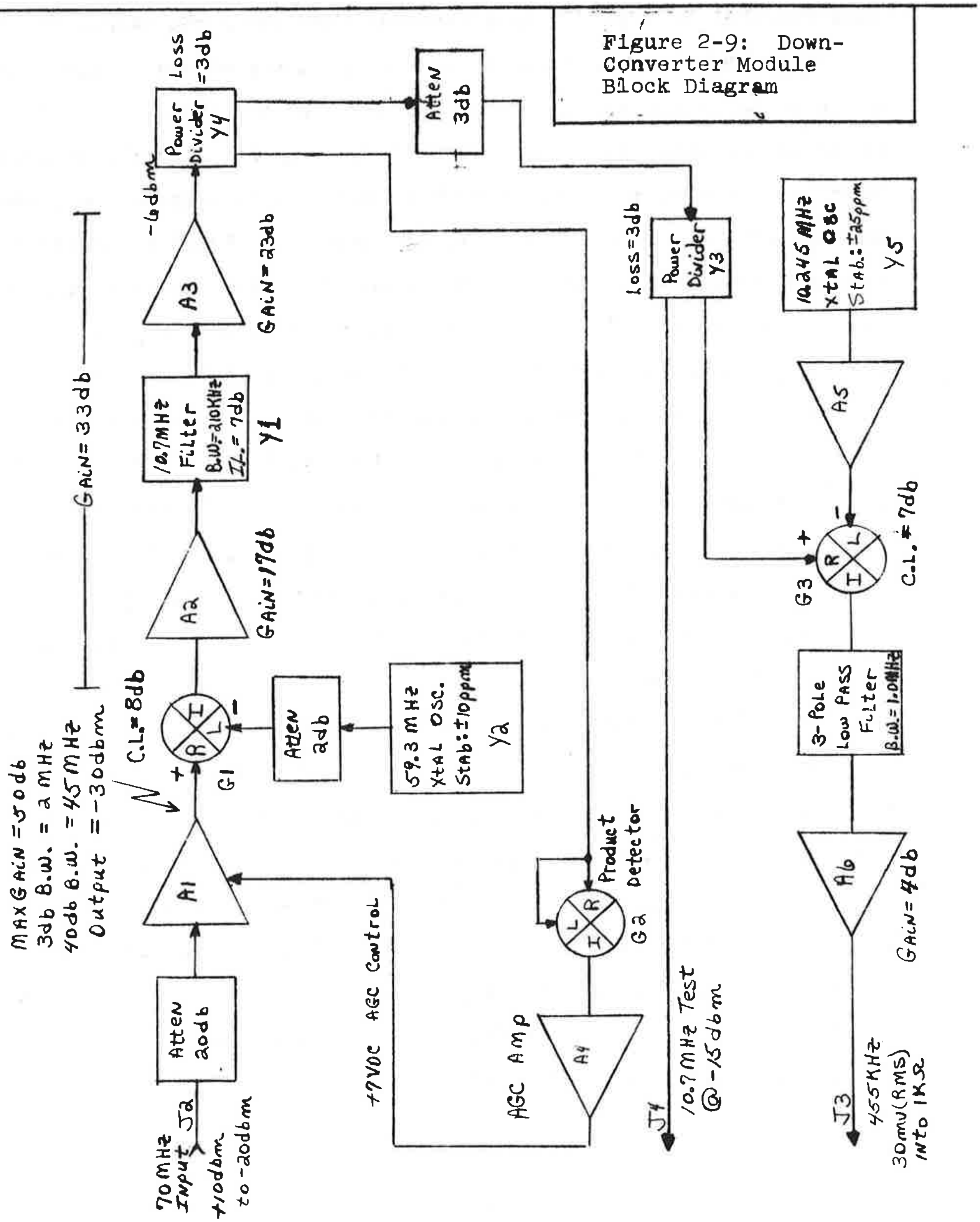


Figure 2-9: Down-Converter Module Block Diagram

control voltage to A1. Since the bandwidth of the detected signal plus noise at 10.7 MHz is much narrower than the 2 MHz bandwidth of A1, it is important to prevent noise overloading at the output of A1. Under no noise conditions the signal level at the input to the R-port of G1 is -30 dBm. At a C/N_O level of 35 dB-Hz the signal plus noise level is -20 dBm, which is 20.0 dB below the 1 dB compression point of amplifier A1 or mixer G1. The 59.3 MHz L.O. signal is derrived from a crystal oscillator Y2. The lower side-band output from G1 is passed through a 10.7 MHz I.F. section, consisting of A2, Y1 and A3. The overall gain at 10.7 MHz is 33 dB and the 3 dB bandwidth is 210 KHz. A ceramic filter determined the overall bandpass response of the 10.7 MHz I.F. section. Filter Y1 provides at least 50 dB rejection at the image frequency of 9.79 MHz. The nominal signal plus noise at the output of A3 is held to a level of -6 dBm by the AGC network. Amplifier A3 is an integrated circuit RF amplifier (UA703), built by Fairchild. The 1 dB compression point for A3 is + 8 dBm. The AGC network is designed to maintain the signal plus noise well below this compression point. The output of A3 is fed through a set of two power dividers to the AGC product detector, the 10.7 MHz front panel test connector and to the 455 KHz down converter. The signal plus noise at 10.7 MHz is fed to mixer G3 where a 10.245 MHz L.O. signal converts the signal to 455 KHz. The L.O. signal is generated by a 10.245 MHz crystal oscillator. The lower side band output from G3 is low pass filtered and then amplified in video amplifier A6. The 455 KHz signal plus noise is then provided as an input to the 455 KHz I.F. and AGC board (A12).

2.2.2 Coherent Demodulator

A block diagram of the Coherent Demodulator is shown in figure 2-10. The Coherent Demodulator is composed of the 455 KHz I.F. & AGC board (A12), the Loop Filter board (A10) and Coherent AGC board (A14). Detailed schematic drawings of boards A10, A12 and A14 are shown respectively in figures 5-10, 5-11, and 5-12 The Coherent Demodulator consists of either a phasellocked loop (PLL) or Costas loop for operation in the Voice or Data mode. The 455 KHz I.F. amplifier, phase detectors and VCO are located on board A12. The loop filter is located on board A10. A coherent AGC network is located on board A14 and is used to maintain a constant level input signal to the coherent demodulator.

In figure 2-10 the 455 KHz signal plus noise is fed through a ceramic filter to I.F. amplifier A1. The bandwidth of the ceramic filter is 40 KHz and is selected to maximize the signal to noise ratio at the phase detectors. Amplifier A1 is a Motorola MC1590G RF amplifier. The gain of A1 is controlled by the Coherent AGC network. The output of A1 is fed to double-balanced mixers, which operate as phase detectors. The coherent reference signals to G1 and G2 are derrived from a 1.82 MHz L.C. VCO and digital quadrature hybrid. The operation of the digital quadrature hybrid is identical to the one described in section 2.1.3 for the Quadrature Modulator. The 1.82 MHz L.C. VCO is designed from an LM375 oscillator network, built by National Semiconductor. The VCO consists of a oscillator network, limiter/buffer network and TTL driver stage. The VCO is designed to have a temperature stability of less than ± 0.4% over a temperature range of 0°C to 50°C. At 455 KHz this results in a frequency instability of ± 1.820 KHz over the temperature range. The combination of VCO frequency instability, Up-Converter and Down Converter frequency

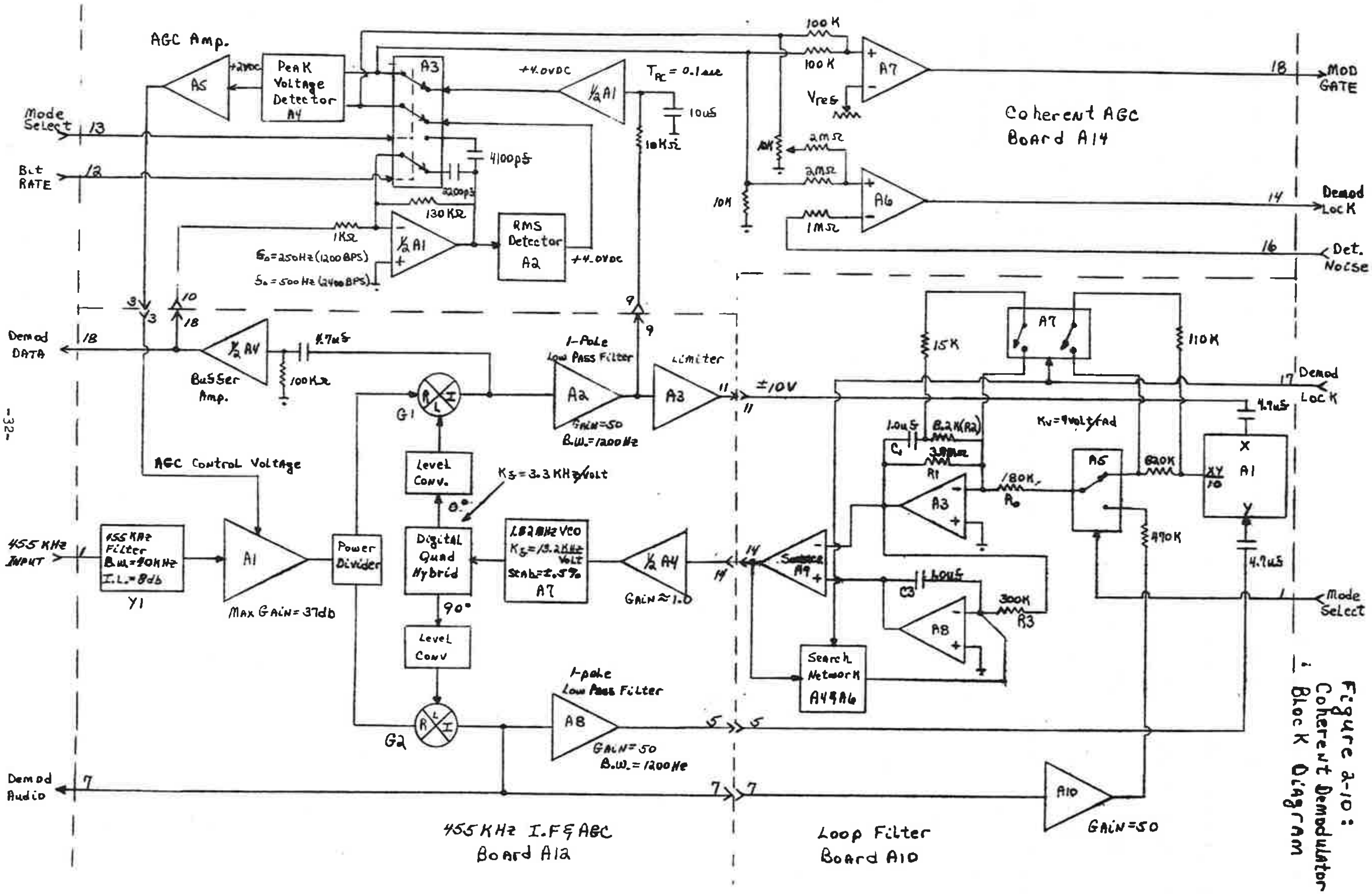


Figure 2-10: Coherent Demodulator Block Diagram

instability, doppler frequency error and L-Band carrier stability determine the frequency search range of the 1.82 MHz VCO. All of the pertinent frequency errors are summarized in Table 2-1.

TABLE 2-1

SYSTEM FREQUENCY ERRORS

Error Source	Max. Frequency Error
Adv. Modem Up-Converter	± 860Hz (0°C to 50°C)
Adv. Modem Down-Converter	± 859HZ (0°C to 50°C)
1.82 MHz VCO (Error at 455 KHz)	± 1.820 KHz (0°C to 50°C)
Doppler Frequency Error	± 1380Hz (600 mph Aircraft)
L-Band Carrier Freq. Error	±1550Hz (± 1 ppm 0°C to 50°C)

Worst Case Frequency Error = ± 6770 Hz

RMS Freq. Error = 2100 Hz

Assuming that all frequency instabilities are independent, the probability of frequency error would follow a Gaussian distribution. If a search range of 2.5 σ (σ = RMS Freq. Error) is chosen, the probability that the frequency error exceeds the ± 5 KHz search range is only 0.5%. This figure is well within the operating requirements of the Advanced Modem equipment.

In figure 2-10, the loop filter configuration is shown. Electronic switches are used to control operation of the loop filter as either a PLL for Voice Only or as a Costas Loop for Data Only and Voice plus Data. An additional electronic switch A7 is used to switch filter components during the acquisition and track modes of operation. During acquisition switcheat A7 are closed, thus shorting a 820K gain resistor and an 8.2 K RC feedback resistor. This operation increases the bandwidth of the loop for fast acquisition. A frequency search network on board A10 provides for sweeping the VCO over a frequency range of ± 5 KHz at a rate of 1 sweep/sec. The loop filter on board A7 is a third order network, where an integrator has been added in parallel with a conventional second order lead-lag loop filter. A third order loop provides for increased performance over a second order loop with respect to static phase error, acquisition range and acquisition time. The open loop transfer characteristic of the loop in figure 2-10 is given as follows:

$$H(S) = \frac{AK_vK_f}{S} \frac{(1 + \tau_2 S)}{(1 + \tau_1 S)} \times \frac{(1 + \tau_3 S)}{\tau_3 S} \qquad (1)$$

where $A =$ D.C. Gain of A3

$\tau_1 = C_1 (R_1 + R_2) = 3.9$

$\tau_2 = C_1 R_2 = .0082$

$\tau_3 = R_3 C_2 = 0.3$

$K_v = 4.0$ volt/rad

$K_f = 3.3$ KHz/volt

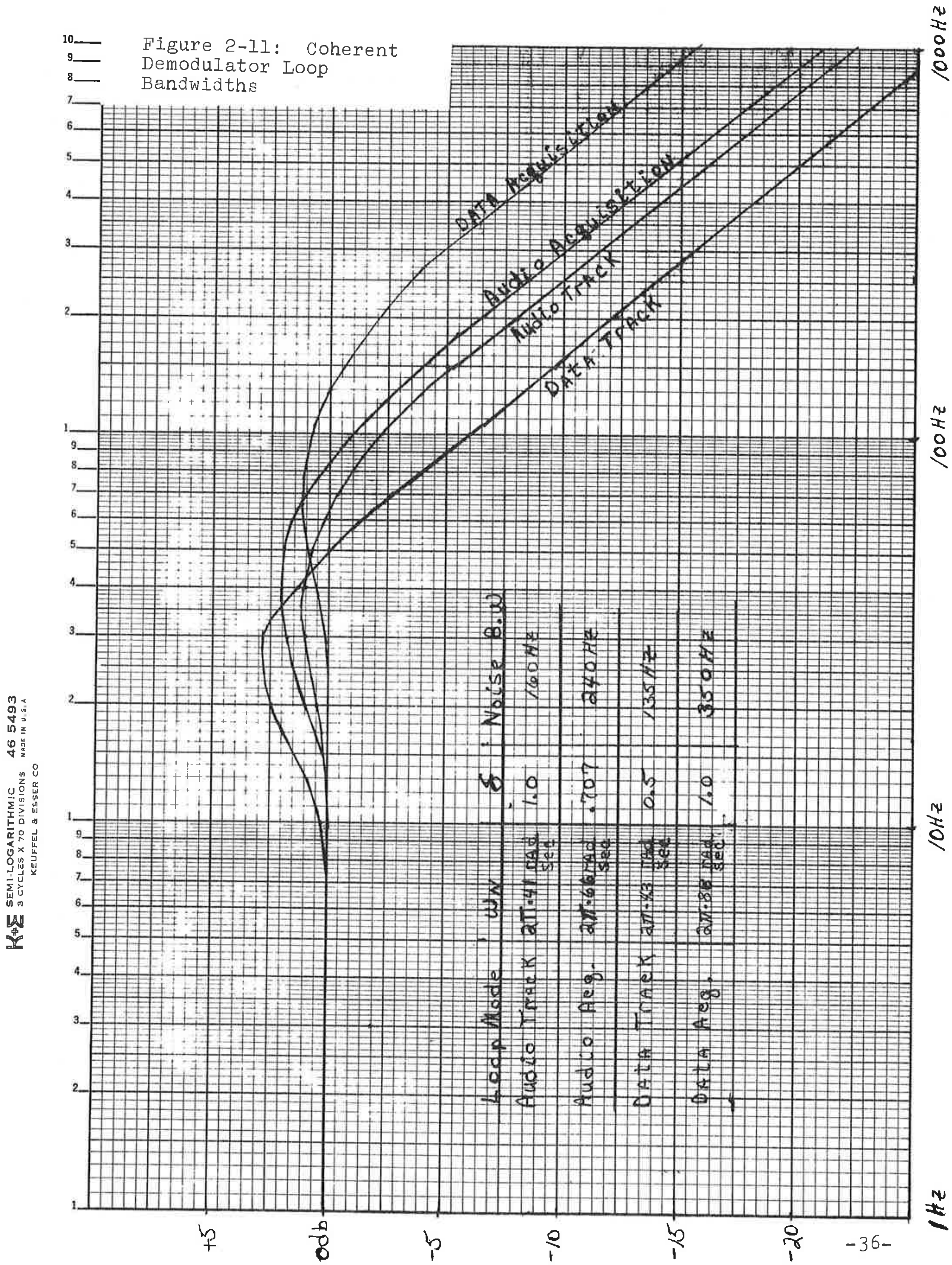
The closed loop response of the loop is given by

$$G(S) = \frac{H(S)}{1 + H(S)} \qquad (2)$$

At the time of acquisition the loop bandwidth of the PLL or Costas Loop is going to be increased due to operation of switch A7 and due to the Coherent AGC network. Since the Coherent AGC operates on detected signal level rather than signal plus noise, prior to signal acquisition the gain of I.F. amplifier A1 on board A12 will be a maximum. At acquisition there will be an increase in signal at phase detectors G1 and G2 and a corresponding increase in phase detector transfer characteristic, K_v. The adaptive increase in signal level at time of acquisition has been measured to be +4 dB above normal input signal, during tracking. The combination of increased K_v, increased loop D.C. gain and increased loop filter lead frequency results in a wide bandwidth for frequency acquisition. After acquisition, the Demod Lock signal opens up switch A7 at board A10 and the loop returns to a narrow band tracking loop. The closed loop response of the PLL and Costas loop are plotted in figure 2-11 for conditions of acquisition and tracking. Also listed in figure 2-11 are the damping factor, natural frequency and noise bandwidth for each loop configuration that is plotted.

In figure 2-10, the frequency search network is shown to work in conjunction with the integrator amplifier, A8, of the loop filter. Prior to acquisition a continuous sawtooth pattern is generated at the output of A8. This sawtooth is generated by applying a low D.C. current +3.3 uA for the 1.0 second sweep period and a high D.C. current -.625 ma for the sawtooth reset period. At the time of signal acquisition a D.C. current equal to and opposite the sweep current is developed at the R3 input resistor to A8. The current at acquisition stops the sweep signal and holds the loop in phase lock. To

Figure 2-11: Coherent Demodulator Loop Bandwidths



counteract the sweep current of +3.3 u amps, an input voltage of +1 VDC is developed at R3. This voltage can be regarded as a static offset voltage needed to counteract the sweep signal. A corresponding phase error at the phase detectors is required to develop this voltage. For a phase transfer characteristic of 4 V/rad at the input to A3 and a D.C. gain of 4.0 at A3, the resulting static phase error is 3.5°. While this static phase error is not large, it would result in a high degree of crosstalk in the Voice plus Data mode. Therefore after acquisition the Demod Lock signal is used to automatically disconnect the Search signal to A8 and thereby remove any static phase error.

The coherent AGC portion of the coherent demodulator is designed to maintain a constant level input signal to the PLL or Costas Loop during carrier tracking periods. In figure 2-10, either the detected carrier portion of the voice signal is fed from A2 (board A12) to board A14 in the voice mode, or the demodulated data signal at A4 (board A12) is fed to A14 in the data mode or voice plus data mode. Electronic switch A3 controls which signal is fed to the AGC control network. In the Voice Mode the detected carrier of the Voice signal is fed through a low pass RC network through A3 to peak voltage detector A4. The detected carrier level is held at +2.0 VDC. However during periods of voice transmission, the power in the carrier drops appreciably. The peak voltage detector, A4, remembers the peak levels during voice transmissions and transmits a continuous +2.0 VDC signal to the AGC feedback amplifier, A5. Incorporation of a peak detector in the AGC provides for a long time constant AGC response on the order of 5.0 seconds. In the data mode the demodulated 1200 BPS or 2400 BPS data signal is fed through a low pass R-C amplifier, A1. The bandwidth of A1 is adjusted according to received bit rate in order to maximize SNR at the output A1. Feedback capacitors are switched across A1 by switch A3 to determine low pass response. The filtered signal from A1 is fed to an RMS detector, A2, which provides a D.C. voltage through switch A3 to peak detector A4. The output level of A2 is held to +4.0 VDC. Also located on board A14, are the Mod Gate and Demod Lock detector networks. At the Mod Gate level detector, A7, the detected Voice carrier or detected data signal is compared against a fixed threshold voltage. During periods of conversation the detected carrier or data signal will drop in voltage, which will in turn be detected by A7. The Mod Gate is then relayed to the C/N_o Monitor board. At the Demod Lock level detector, A6, the detected voice carrier or demod data is compared against the detected noise level from the C/N_o Monitor Network. At board A8 the demodulated noise is filtered in a 7200 Hz bandpass filter and then detected. Prior to signal reception, the level of detected noise exceeds the detected signal level and the Demod Lock signal is a logic "0". Upon carrier acquisition, the detected signal level exceeds the detected noise level and the Demod Lock signal is a logic "1".

2.2.3 C/N_o Measurement

A block diagram of the C/N_o Monitor board, A8, and panel test meter is shown in figure 2-12, and a detailed schematic drawing of board A8 is shown in figure 5-13. In figure 2-12 the demodulated audio signal plus noise is fed to bandpass filter A1. The filter is designed to accept a band of noise about 7200 Hz and reject lower frequency voice signals. Amplifier A1 is an active filter network with a Twin-T

C/No	RMS Noise	D.C. Voltage	Log Amp Out	A6 Output	Current
35db-Hz	1V (RMS)	1V DC	-2.0VDC	0 VDC	0 mA
45db-Hz	.316 V (RMS)	.316 VDC	-1.0 VDC	-1 VDC	-0.5 mA
55db-Hz	.1 V (RMS)	.1 VDC	0 VDC	-2 VDC	-1.0 mA

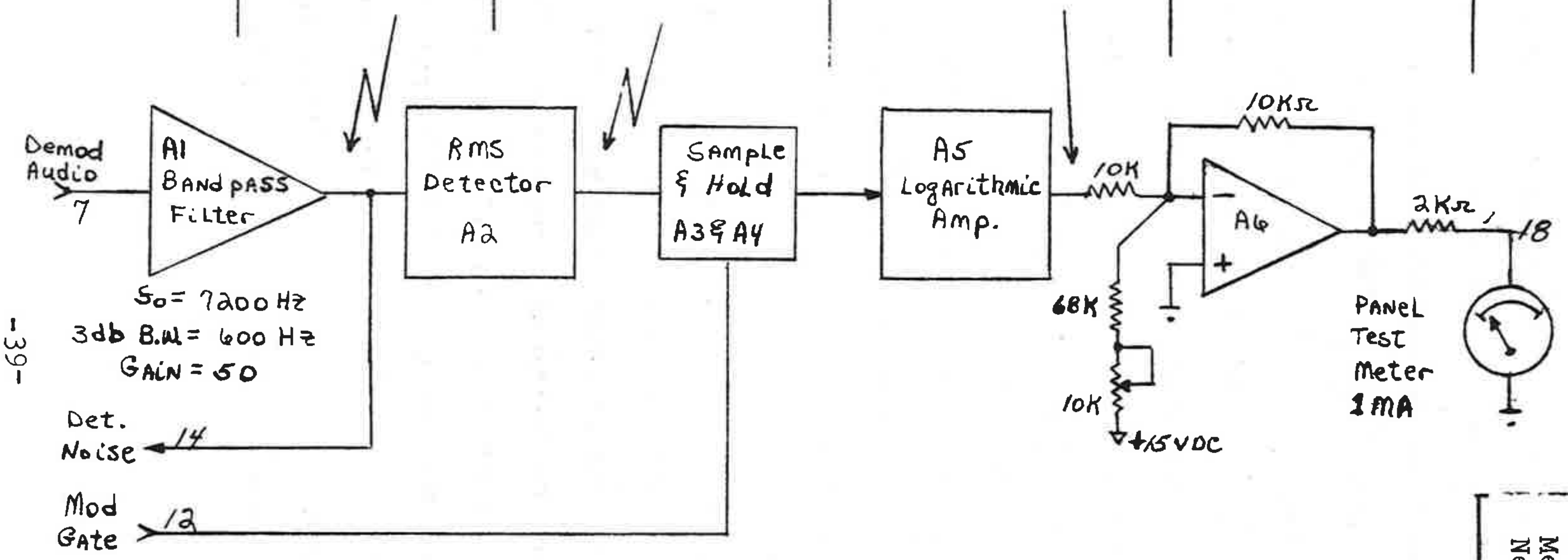


Figure 2-12: C/N_o Measurement Network Block Diagram

feedback netowrk. The filtered noise from A1 is fed to an RMS voltage detector. The detected D.C. noise voltage is fed through a sample and hold network to log amp A5. The sample and hold network stores the detected noise voltage during periods of voice transmission, thus rejecting further any voice power from the C/N_o measurement. The output D.C. voltage from log amp A5 is given as follows:

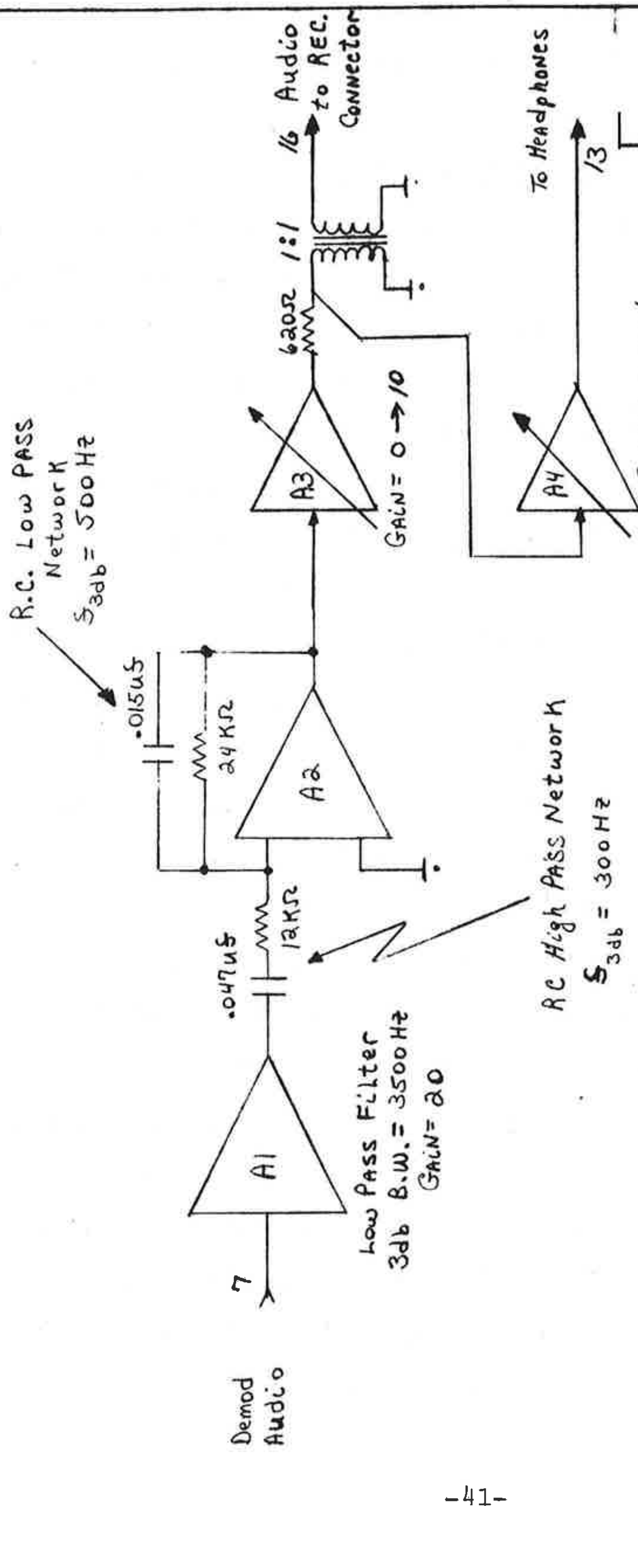
$$V_{out}\ (A5) = -\left[2 \log (V_{in}) \right] \text{-VDC} - 2.0\ \text{VDC} \qquad (3)$$

The converted log voltage is fed through op amp A6 to the front panel current meter. A voltage trim adjust is provided at A6 for calibrating the front panel meter. Operation of the C/N_o measurement network depends on the fact that the Coherent AGC Network is holding the signal level constant over the range of C/N_o signal levels. For any increase or decrease in C/N_o there is a corresponding change in noise power while the signal level remains constant. The C/N_o network measures the change in noise power and converts the measured level to logarithmic function for display on the front panel meter.

2.2.4 Audio Processing

A block diagram of the Audio Processor is shown in figure 2-13 and a detailed schmeatic diagram of board A6 is shown in figure 5-14. The demodulated audio signal is passed through a 3500 Hz low pass filter, A1, and then fed to de-emphasis network A2. Low pass filter A1 restricts the received noise to a bandwidth no greater than the audio transmission bandwidth, thus optimizing voice signal SNR. A high pass RC network is situated at the input to amplifier A2 and is used to eliminate noise components below 300 Hz; again this improved signal SNR. The voice signal is de-emphasized at A5 at a rate of -6 dB/octave

Figure 2-13: Audio Processor Block Diagram



from 500 Hz to infinity. The deeemphasis response is matched to the pre-emphasis response at the modulator. Two variable gain amplifiers are provided at the audio processor to drive either tape recording equipment or monitor headphones.

2.2.5 Data Decoder and Clock Synchronization

A block diagram of the Data Decoder is shown in figure 2-14. The Data Decoder consists of an Integrate and Dump matched filter, which optimally filters the received data prior to level detection. The I&D Network is located on board A4. A maximum likelihood level decision is made at the end of each integration period prior to dumping the integrator. Clock synchronization for operation of the I&D network is generated on board A3. Detailed schematic drawings of boards A4 and A3 are shown respectively in figures 5-15 and 5-16.

In figure 2-14 the demodulated data is fed through amplifier A1 (Bd A4) to I&D networks #1 and #2. The data is amplified to a level of 0.8 volt (P-P) at the output of A1. A waveform diagram, showing the operation of the Data Decoder, is contained in figure 2-15. At I&D network #1 the received data bit is integrated over the full bit period. At I&D network #2 the data is first chopped by the locally generated clock. The chopping procedure results in a signal inversion half-way through each bit period. While the output of I&D #1 integrates to some positive or negative level at the end of each bit period, the output of I&D #2 integrates to zero volts over each bit period. At the end of each bit period a level detector is used to determine the polarity of each I&D network. The output of I&D #1 is the received data signal and it is fed through a two stage shift register, A10, whose parallel outputs are differentially decoded in an exclusive "OR" network. The decoding sequence is as follows:

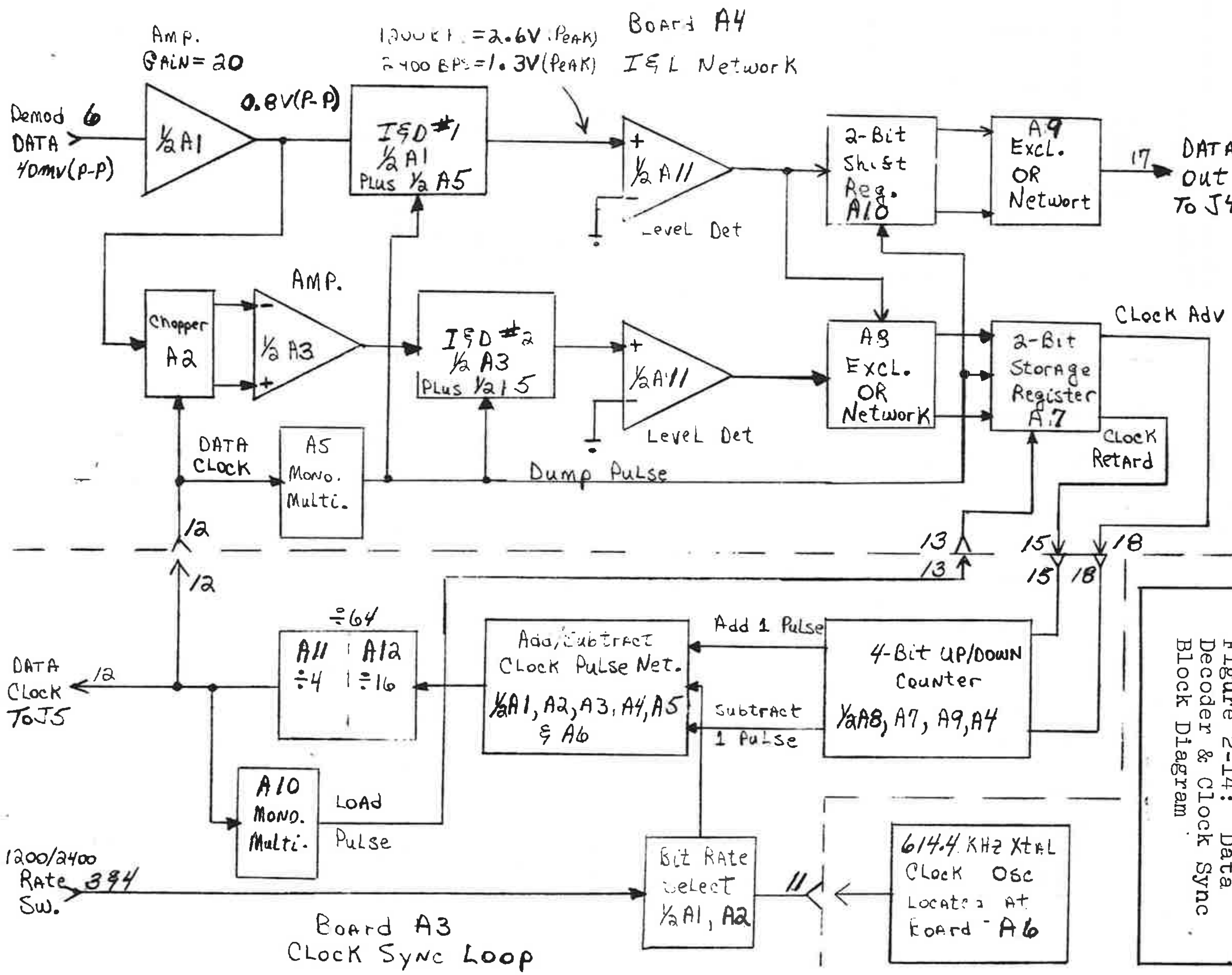
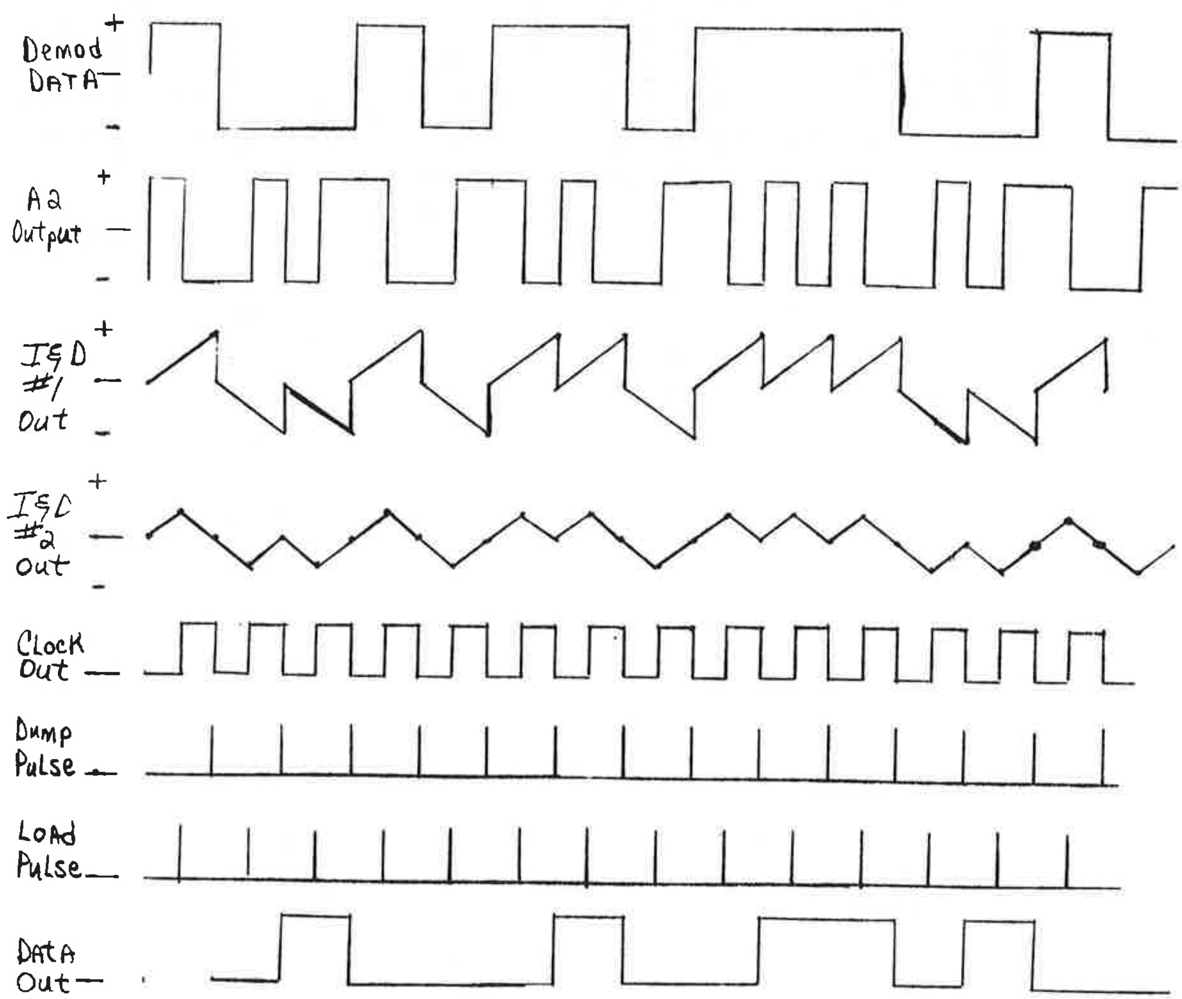


Figure 2-14: Data Decoder & Clock Sync Block Diagram

Figure 2-15: Waveform Timing Diagram



Bit_N	Bit_{N-1}	Output at EXCL OR
0	0	0
0	1	1
1	0	1
1	1	0

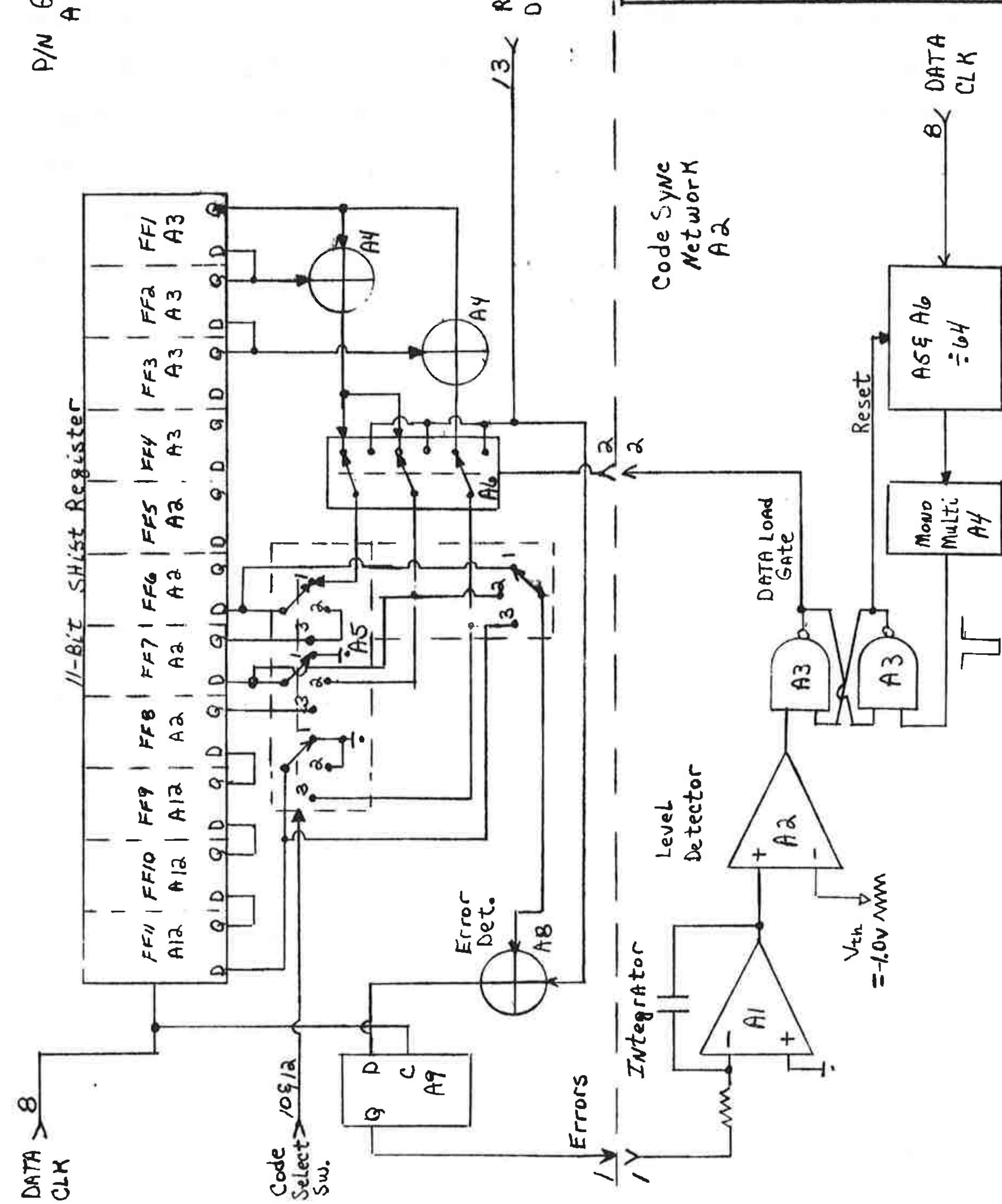
The polarity of the output signal from I&D #2 is also detected at A11. Normally, if the local clock is in bit synchronization with the received data, the output of A3 will integrate to zero volts during each bit period. However, if the local clock leads or lags the received data stream, then the output of I&D #2 will integrate to some positive or negative voltage. The polarity of I&D #2 is compared in an exclusive OR network, A8, against the polarity of I&D #1. It can be seen from figure 2-15 that if the local clock lags the received data, the polarity of the I&D networks are opposite, and a clock advance signal will be stored in the two bit storage register A7. Similarly, if the local clock leads the received data the polarity of the two I&D networks are the same, and a clock retard signal is stored in the two bit storage register, A7. In the middle of each bit period the contents of the storage register are loaded into a 4 bit up-down counter. When the counter accumulates a unanimous count of all 1's or all 0's, a phase step is added to or subtracted from the local clock. At the same time the up-down counter is reset to an initial count of 1000, and it begins to accumulate advance or retard counts again.

The size of the clock phase step is determined by the division ratio for the local clock. For 1200 BPS operation, the 614.4 KHz crystal clock is divided-by-4 to generate a 153.6 KHz reference, which is sent to the ADD/SUBTRACT Clock Pulse Network. Under normal conditions the 153.6 KHz clock is divided by 2 and then by 64 to generate a 1200 Hz clock signal. Phase steps at 1/64 the bit period are added to or subtracted from the resulting 1200 Hz clock. For 2400 BPS operation, the 614.4 KHz crystal oscillator signal is divided-by-2 and fed to the ADD/SUBTRACT network, where again 1/64 phase steps are added to or subtracted from the local clock. The 1/64 phase steps corresponds to discrete phase increments of about 5.6°. The advancing or retarding of the local clock in discrete steps, keeps this clock in bit synchronization with the received data.

2.2.6 Code Synchronization and Error Detector

A block diagram of the Code Synchronizer and Bit Error Detector is shown in figure 2-16. The Code synchronizer consists of a local code generator which generates P/N codes identical to the codes generated at the Modulator. This code generator is synchronized with the received data sgream such that bit error detection is possible. Detailed schematic diagrams of the Code Sync Network (Bd.A2) and the P/N Generator (Bd.A1) are shown in figures 5-17 and 5-18, respectively.

Figure 2-16: Code Sync and P/N Generator Block Diagram



In figure 2-16 the bit synchronized data clock and received data are connected to board A1. At board A1, an 11 bit shift register generates any of three codes which are identical to the three P/N codes transmitted by the Advanced Modem Modulator. If the Received Data Code is in synchronism with the local code, then error detection can be performed at A8 and A9. The detected errors are fed to an integrator, A1, on board A2. If the error rate approaches 50%, then A1 will integrate to a negative value and trip the level detector A2. A2 will in turn drive latch network A3, which will generate a LOAD GATE to switch A6 on board A1. While the Load Gate is low, A6 will switch received data into the 11-Bit shift register. At this time the received data is being compared against itself at the error detector and no errors are loaded into the integrator. The output of A1 will thus return to zero. The load gate will remain low for a period of 64 clock pulses as counted at A5 and A6 on board A2. At the end of this 64 clock pulses, monstable multivibrator A4 will be triggered and the latch network will be reset. The Load Gate will now go high. At this time the state of the 11 bit shift register has been preset by loading in received data. If eleven consecutive bits have been received and loaded into the shift register without error then the shift register will continue generating the P/N sequence without error. The received data and P/N sequence generator are now synchronized. If eleven bits are not loaded in correctly, then the sync network will continue the above process until code sync is achieved. At received C/N_o levels of about 37 dB-Hz the error rate approaches 10^{-2}. The probability of error in loading eleven bits correctly is 10^{-1}. So there is 90% probability of success at 37 dB-Hz of synchronizing the P/N code on the first attempt.

Not shown in the block diagram of figure 4-18 are the output networks for various signals which are connected to the front panel RECORDER connector. The output signals are provided at discrete levels of 0V to +1V at an output impedance level of 150 Ω. These signals from board A2 are listed as follows: DATA, DATA CLOCK, ERRORS, MOD GATE.

3. SYSTEM TEST RESULTS

Acceptance Testing of Hybrid Modem #1 Systems #1 and #2 were performed at Bell Aerospace from January 28, 1974 to January 30, 1974. These tests were made to demonstrate compliance of the Hybrid Modem Equipment to DOT-TSC contract specifications (Contract No. DOT-TSC-631, Exhibit A) and to determine the overall performance of the Hybrid Modem System under specific test conditions. Tests were made to determine system Voice Intelligibility (see Table 3-1), data error rate performance and carrier acquisition performance. As part of the Voice Intelligibility testing pre-recorded tapes, supplied by DOT-TSC, were played throughthe Hybrid Modem Systems under varying C/N_o conditions and the results recorded. The recorded tapes were delivered to CBS Labs for evaluation. Voice intelligibility results are presented in Table 3-2 and Figure 3-1.

3.1 Voice Intelligibility Tests

The voice intelligibility performance of the Hybrid Modem was tested with the Harvard PB-50 word list. Pre-recorded tapes of the Harvard PB-50 word list were delivered by DOT to Bell Aerospace for Acceptance Testing of the Hybrid Modem. A total of sixteen tapes were provided to the performance of the tests. Each tape contained 500 words or 10 lists of 50 words/list. A total of four separate speakers were used in recording the tapes. There were two male and two female speakers, and each speaker was recorded on four tapes. The PB-50 word list consists of 1000 words. For these acceptance tests four lists were used with different scramblings.

The test conditions under which the voice tests were made are listed in Table 3-1. For each test condition a total of 500 words were recorded through the system. Respective word lists for each test condition are listed in Table 3-1.

TABLE 3-1

VOICE INTELLIGIBILITY TEST CONDITIONS

Modem Unit	C/No	Transmit Mode	Voice Tape
S/N 1	46 db-Hz	Voice Only	4E2
S/N 1	43 db-Hz	Voice Only	2F2 & 4D2
S/N 1	40 db-Hz	Voice Only	3F1
S/N 1	37 db-Hz	Voice Only	1G1
S/N 1	49 db-Hz	Voice plus Data	4E1
S/N 1	46 db-Hz	Voice plus Data	2F1 & 4D1
S/N 1	43 db-Hz	Voice plus Data	3E2
S/N 1	40 db-Hz	Voice plus Data	1F2
S/N 2	46 db-Hz	Voice Only	4D2
S/N 2	43 db-Hz	Voice Only	2E2 & 4E2
S/N 2	40 db-Hz	Voice Only	3E1
S/N 2	37 db-Hz	Voice Only	1F1
S/N 2	49 db-Hz	Voice plus Data	4D1
S/N 2	46 db-Hz	Voice plus Data	2E1 & 4E1
S/N 2	43 db-Hz	Voice plus Data	3D2
S/N 2	40 db-Hz	Voice plus Data	1E2

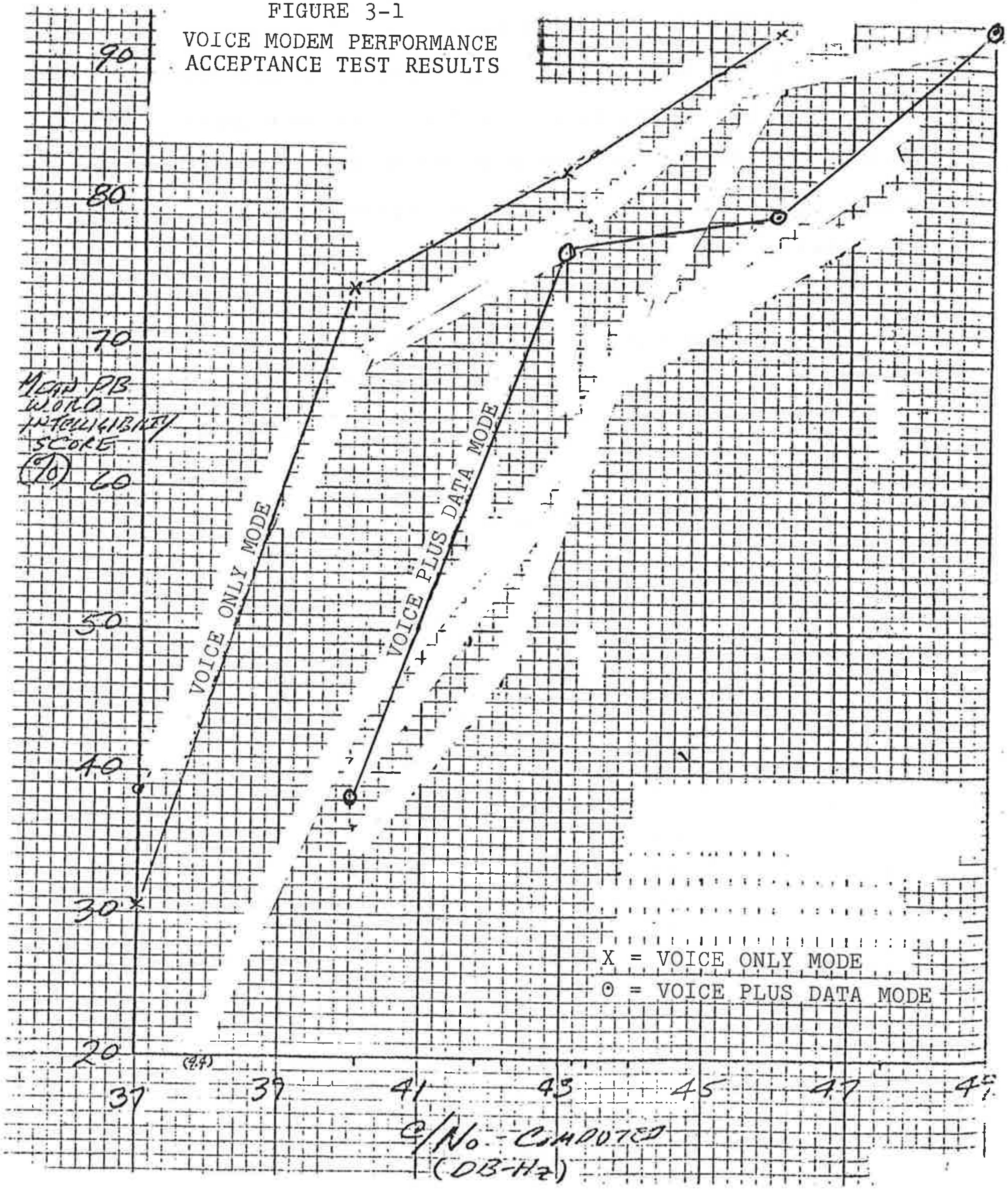
In table 3-1 it is noted that an additional 500 words were recorded at a C/No level of 43 db-Hz in the Voice only mode and at 46 db-Hz in the Voice plus Data mode. The additional words were recorded to test any differences in the scoring performance of female versus male speakers. Tapes 2F2, 2F1, 2F2 and 2E1 were recorded by a female speaker, while tapes 4D2, 4D1, 4E2 and 4E1 were recorded by male speaker. The recorded tapes were delivered to CBS Labs on February 5, 1974 for scoring and evaluation. The results of these tests were reported to DOT-TSC by CBS Labs, and these results will be a part of the final acceptance test data for the Hybrid Modem System. A summary of the acceptance test results is presented in Table 3-2 and Figure 3-1.

TABLE 3-2

SUMMARY ACCEPTANCE TEST RESULTS
Q-MOD/PSK HYBRID MODEM - S/N/

C/No (DB-Hz) [Meter Reading]	MEAN INTELLIGIBILITY SCORE (PER CENT) Voice Only Mode	Voice Plus Data Mode
37	30.5	No Meas.
40	74.0	38.2
43	82.1	76.6
46	92.4	79.3
49	No Meas.	92.9

FIGURE 3-1
VOICE MODEM PERFORMANCE
ACCEPTANCE TEST RESULTS



3.2 Data Error Rate Tests

The data error rate performance of each Hybrid Modem system was tested as part of the acceptance tests. Error rates were tested in the data mode and data plus voice mode over a range of C/No values. The test conditions for each system are listed in Table 3-3.

TABLE 3-3

DATA ERROR RATE TEST CONDITIONS

Xmit Mode	Bit Rate	C/No	No. of Bits Xmit	Time Period	Voice Signal
Data	1200 BPS	37 db-Hz	7.2×10^4	1 min	N.A.
		40 db-Hz	7.2×10^5	10 min	N.A.
		42 db-Hz	43.2×10^5	60 min	N.A.
	2400 BPS	40 db-Hz	14.4×10^4	1 min	N.A.
		43 db-Hz	7.2×10^5	5 min	N.A.
		45 db-Hz	43.2×10^5	30 min	N.A.
Data Plus Voice	1200 BPS	40 db-Hz	7.2×10^4	1 min	Tape 4E2
		43 db-Hz	7.2×10^5	10 min	Tape 4E2
		45 db-Hz	43.2×10^5	60 min	Tape 4E2
	2400 BPS	43 db-Hz	14.4×10^4	1 min	Tape 4E2
		46 db-Hz	7.2×10^5	5 min	Tape 4E2
		48 db-Hz	43.2×10^5	30 min	Tape 4E2

The theoretical performance of a coherent phase shift keyed communication system with differential encoding is given by the following equation:

$$P_E = 1 - ERF(E_b/N_o)^{1/2} \qquad (4)$$

where E_b/N_o = Engery-per-bit to noise spectral density ratio

and C/No (in db) = E_b/N_o (in db) + Bit Rate (in db)

The theoretical performance for each bit rate and each system is plotted in Figures 3-2 and 3-3. Plotted in each figure are the test results recorded during acceptance testing. The results of error rate tests in the Data mode and Data plus Voice mode are plotted on a common graph. The performance specification calls out that the error rate be less than 10^{-5} at a C/N_o of 42 db-Hz and a bit rate of 120 BPS in the Data Only mode. This specification provides a 1.3 db margin at 42 db-Hz above theoretical performance. This 1.3 db margin is extrapolated to the entire curve at 1200 BPS and is also applies to the 2400 BPS error curve. No theoretical curve is drawn for the Data plus Voice mode because of the difficulty in analyzing the periodic nature of the communication channel. The random nature of the voice signal bars any practical analysis of its effects on data error rates. There is a performance specification for the Voice plus Data mode that calls for error rates less than 10^{-5} at a C/N_o of 45 db-Hz at 1200 BPS and at a C/N_o of 48 db-Hz at 2400 BPS. In Figures 3-1 and 3-2 it is seen that all error rates fall within equipment performance specifications.

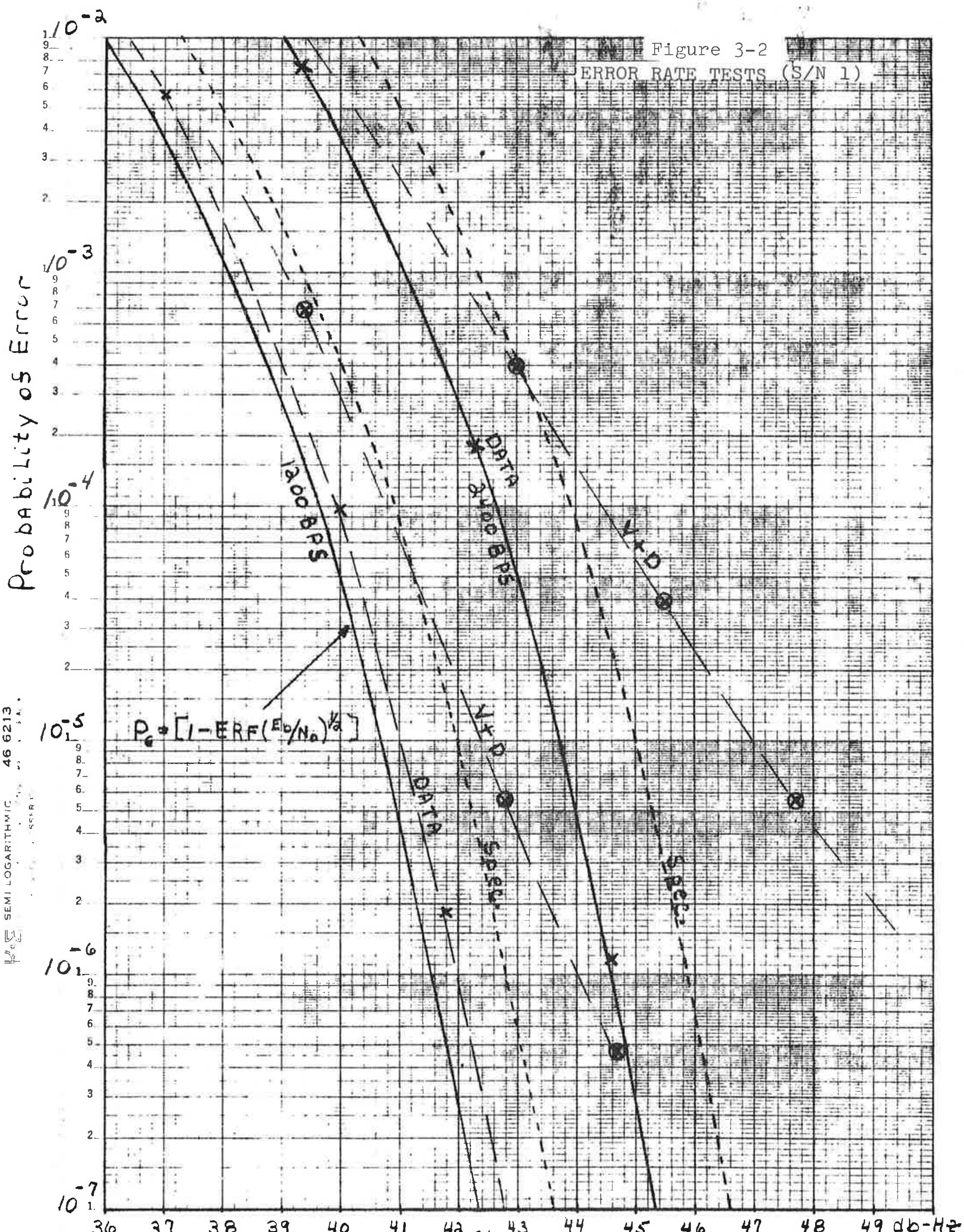


Figure 3-2

ERROR RATE TESTS (S/N 1)

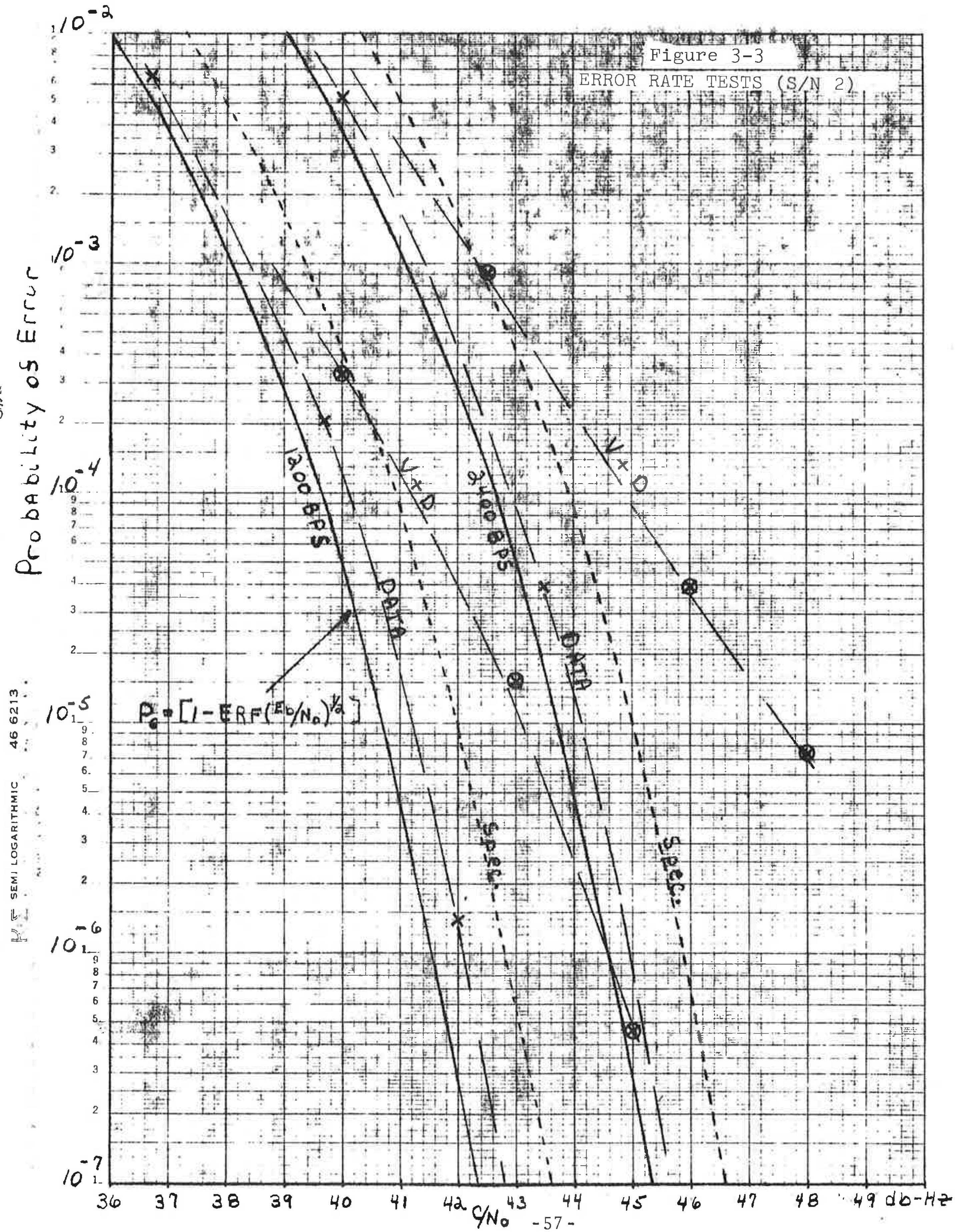


Figure 3-3
ERROR RATE TESTS (S/N 2)
Probability of Error
1200 BPS
2400 BPS
V + D
V + D
DATA
DATA
SPEC.
SPEC.
$P_e = [1 - ERF(E_b/N_o)^{1/2}]$
C/No
db-Hz
SEMI LOGARITHMIC 46 6213

3.3 Carrier Acquisition

The Hybrid Modem Demodulator is required to provide rapid carrier acquisition in the three operating modes of Voice only, Data only and Voice plus Data. Acquisition is required over a carrier frequency error of ±4 KHz and down to C/N_o levels of 37 db-Hz. For all acquisition conditions an acquisition time of less 1.0 second is required. The specified acquisition test conditions are listed in Table 3-4.

TABLE 3-4

ACQUISITION TEST CONDITIONS

Xmit Mode	C/N_o	Frequency Error	Acquisition Time	Bit Rate	Voice Source
Voice Only	37 db-Hz	±4 KHz	$<$1.0 second	N.A.	Tape 4E2
Data Only	37 db-Hz	±4 KHz	$<$1.0 second	1200 BPS	N.A.
Data plus Voice	40 db-Hz	±4 KHz	$<$1.0 second	1200 BPS	Tape 4E2

As described in section 2.2.2 on the Coherent Demodulator, the search range for the Demodulator is ±5 KHz which exceeds the required ±4 KHz search range. The range of frequency instabilities dictated that a ±4 KHz search range did not adequately provide for all possible frequency errors. Therefore, the Hybrid Modem Demodulator sweep range was increased to ±5 KHz. All acquisition tests were performed for a sweep range of ±5 KHz. Prior to carrier acquisition the demodulator continuously sweeps over the expected frequency range of the received carrier (70 MHz ±5 KHz). The sweep signal is a sawtooth waveform with a sweep period of 1.0 second. A carrier signal may be received randomly at any time point in the 1.0 second sweep period. Acquisition time will depend on carrier frequency error and the time point of carrier reception with respect to the sweep signal. Acquisition time may be as small as 100 msec or as long as 1.0 sec. In no case should the acquisition time exceed 1.0 second for in that case, the demodulator will have skipped a sweep cycle in the process of acquisition. A successful acquisition is defined as carrier acquisition within one period of the sweep signal. An unsucessful acquisition is defined as a carrier acquisition which exceeds one period of the sweep signal.

In addition to the acquisition tests performed under the conditions listed in Table 3-3, the drop lock point of the demodulator was measured with respect to signal C/N_o for the three modes of operation. The drop lock point is defined as the lowest C/N_o level at which the Demodulator will maintain phase lock. The acquisition test results are listed in Table 3-5.

From Table 3-4 it is seen that the acquisition range in the Data and Data plus Voice mode was not tested. Rather, it is inferred from the Voice only acquisition range test, that since the sweep range in the Voice mode and Data mode are identical, the acquisition range in each mode is identical. The minimum acquisition C/N_o level for the Data mode at 2400 BPS was not tested because there is no acquisition specification at this data rate. Lab tests confirm, however, that the acquisition performance in the data mode at 2400 BPS is identical to the operation at 1200 PBS.

In Table 3-4 it is specified that the Hybrid Modem Demodulator, while operating in the DATA mode, acquire the DCPSK carrier at a C/N_o of 37 db-Hz within 1.0 second over a carrier frequency error of ± 4 KHz. The Test Results of Table 3-5 show that the minimum C/N_o acquisition level in the Data Mode was 37.8 db-Hz for both systems. At a C/N_o of 37 db-Hz, neither system was able to acquire within 1.0 second. Rather, two or three sweep periods were required for acquisition at a C/N_o of 37 db-Hz. This failure to meet specification is not considered a liability in terms of system operation. At a C/N_o of 38 db-Hz the data error rate is greater than 10-3 for bit rates of 1200 BPS. At these particular error rates the usefulness of the data schannel is questionable.

TABLE 3-5

ACQUISITION TEST RESULTS

Unit S/N	Xmit Mode	C/N_o Acq. Level	Freq. Acq. Range	Sweep Period	Acq. Time	Drop Lock Point	Data Rate	Voice Source
S/N 1	Voice	37 db-Hz	69.996 MHz to 70.004 MHz	1.06 sec	<1.0 sec	32 db-Hz	N.A.	Tape 4E2
S/N 1	DATA	37.8 db-Hz	Not tested	1.0 sec	<1.0 sec	34 db-Hz	1200 BPS	N.A.
S/N 1	DATA	Not tested	Not tested	1.0 sec	<1.0 sec	33 db-Hz	2400 BPS	N.A.
S/N 1	Voice plus Data	39.8 db-Hz	Not tested	1.0 sec	<1.0 sec	34 db-Hz	1200 BPS	Tape 4E2
S/N 2	Voice	36.7 db-Hz	69.996 MHz to 70.004 MHz	0.8 sec	<1.0 sec	31 db-Hz	N.A.	Tape 4E2
S/N 2	DATA	37.8 db-MHz	Not tested	0.9 sec	<1.0 sec	35 db-Hz	1200 BPS	N.A.
S/N 2	DATA	Not tested	Not tested	0,9 sec	<1.0 sec	34 db-Hz	2400 BPS	N.A.
S/N 2	Voice plus Data	40 db-Hz	Not tested	0.9 sec	<1.0 sec	36 db-Hz	1200 BPS	Tape 4E2

4. C/N_o CALIBRATION

The Hybrid Modem Demodulator provides a direct reading panel meter for C/N_o measurement. This meter has been calibrated at Bell Aerospace prior to system delivery. The panel meter reads the total received signal C/N_o in db-Hz steps from 35 db-Hz to 55 db-Hz and operates in all three modes of operation: Voice only, Data only and Voice plus Data. Provision is made for external calibration of the C/N_o meter by standard test equipment, and calibration may be performed during normal operation of the equipment.

For laboratory operation, the equipment test setup of Figure 4-1 may be used for calibration of the Demodulator C/N_o meter. Hewlett-Packard 462A wideband amplifiers are used as 70 MHz noise sources. The wideband noise is filtered in a 70 MHz bandpass filter (3 db B.W. = 4.0 MHz) and then amplifier by an H-P 461A amplifier to a power level of about -3 dbm. The bandpass gaussian noise is then summed with the signal from the modulator. Attenuators at the modulator output provide for adjustment of the signal-to-noise ratio to the demodulator. The 70 MHz signal plus noise to the demodulator is down-converted to 10.7 MHz at the Hybrid Modem Demodulator and is provided at the front panel 10.7 MHz test connector. The C/N_o of the received signal may be measured on a H-P 312A selective voltmeter at the 10.7 MHz test connector. The following calibration procedure is outlined:

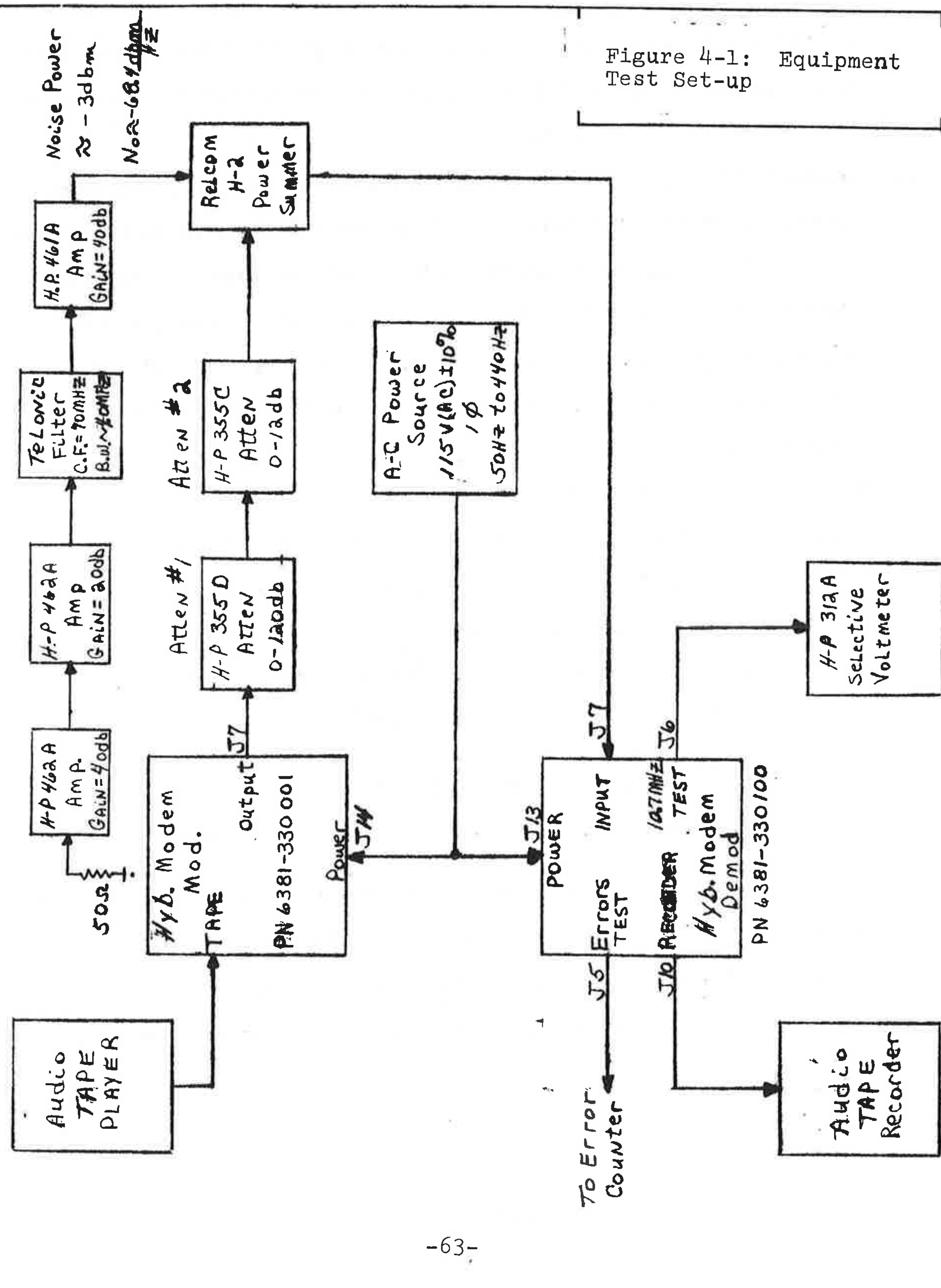


Figure 4-1: Equipment Test Set-up

a. Set the MODE SELECT switches of the modulator and demodulator to the VOICE position and verify the DEMOD LOCK indicator lights. Set ATTENUATORS #1 and #2 of Figure 4-1 such that the demodulator C/N_o meter reads 45 db-Hz.

b. Connect the H-P 312A Selective Voltmeter to the 10.7 MHz test connector at the demodulator. Tune the H-P 312A to the 10.7 MHz carrier frequency and measure and record the signal voltage. Offset the H-P 312A by 5 KHz from the carrier frequency and measure and record the noise voltage. The H-P 312A should be set to a measurement bandwidth of 200 Hz for each voltage measurement.

c. The C/N_o of the received signal may be calculated from the recorded readings. Since the 312A Selective Voltmeter is an average reading device, the true RMS noise voltage is 1 db higher than the recorded reading. The noise bandwidth of the H-P 312A is 200 Hz (23 db). From this data the signal C/N_o can be calculated from the following equation:

$$C/N_o = \text{Signal (in db)} - \text{Noise (in db)}$$
$$\text{10 db (Avg. to RMS correction)} + \text{23 db (Noise B.W.)}. \quad (5)$$

d. Verify the C/N_o meter reading at the demodulator agrees with the H-P 312A measured C/N_o within ±0.5 db. If the C/N_o meter is out of calibration, the meter may be set to the correct reading by adjustment of potentiometer P2 on board A8 (C/N_o Monitor).

e. Measure and record respective C/N_0 meter readings and H-P 312A Selective Voltmeter readings over a range of 37 db-Hz to 51 db-Hz in 2 db-Hz steps. At each C/N_0 level record the settings of ATTENUATORS #1 and #2 of Figure 4-1.

f. Data Only Calibration - Set the MODE SELECT switch to the DATA position at the modulator and demodulator units. Set the BIT RATE switches to 1200 BPS. Set the DATA SELECT switches to INT 3. For the attenuator settings of the previous paragraph record the respective C/N_0 meter readings. Reset the BIT RATE switches to 2400 BPS and record the C/N_0 readings for the range of attenuator settings.

A calibration of each Hybrid Modem Demodulator was performed as part of the Acceptance Test procedure. The results of these calibrations are plotted in Figure 4-2 and 4-3. In each figure the front panel C/N_0 meter reading is plotted against the H-P 312A Selective Voltmeter Measurement. A typical data sheet which may be used in recording C/N_0 calibration data is shown in Figure 4-4. Regular calibration of the Hybrid Modem C/N_0 network is recommended to assure reliable operation of the equipment.

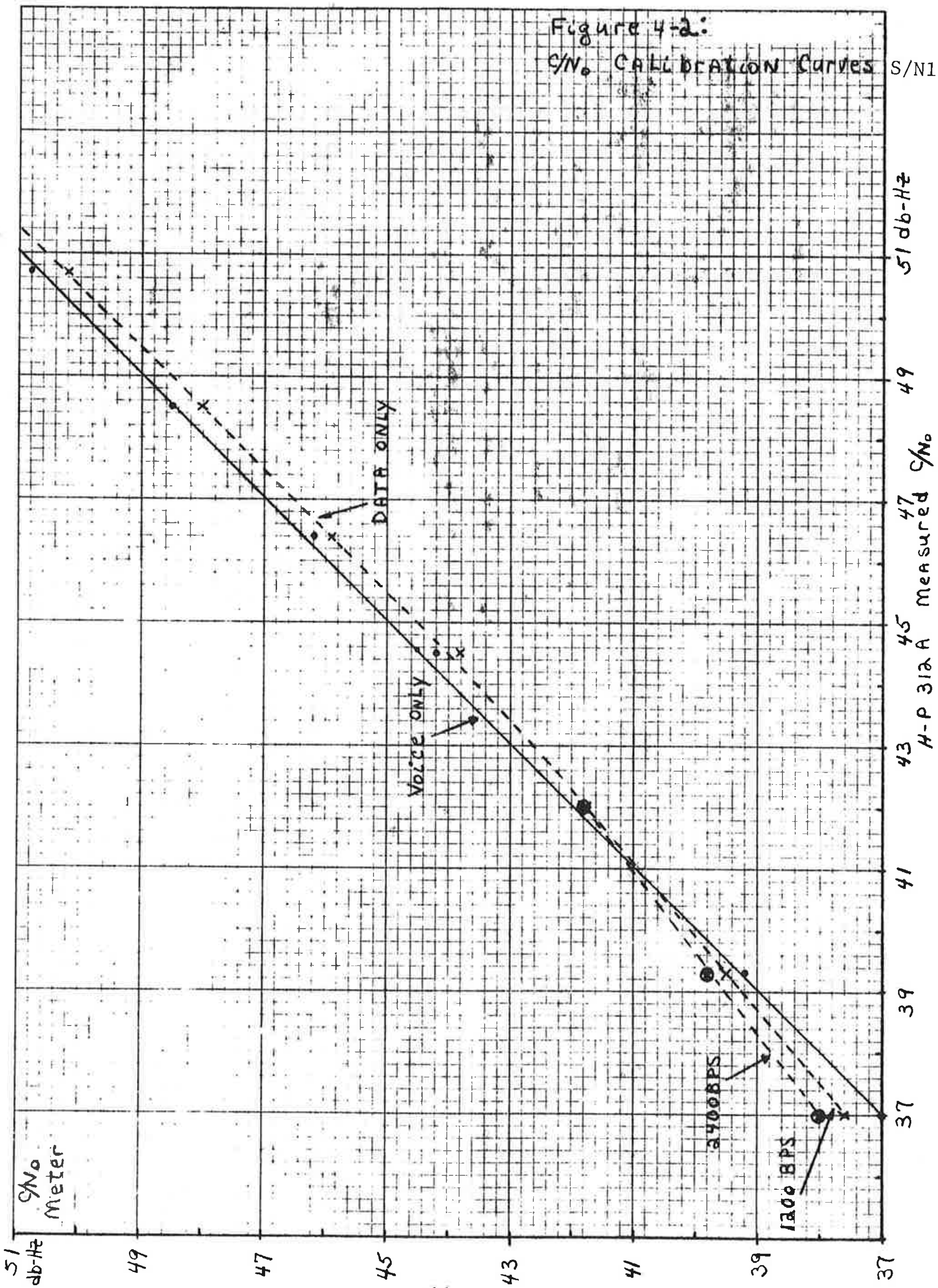


Figure 4-2: C/No CALIBRATION Curves

S/N1

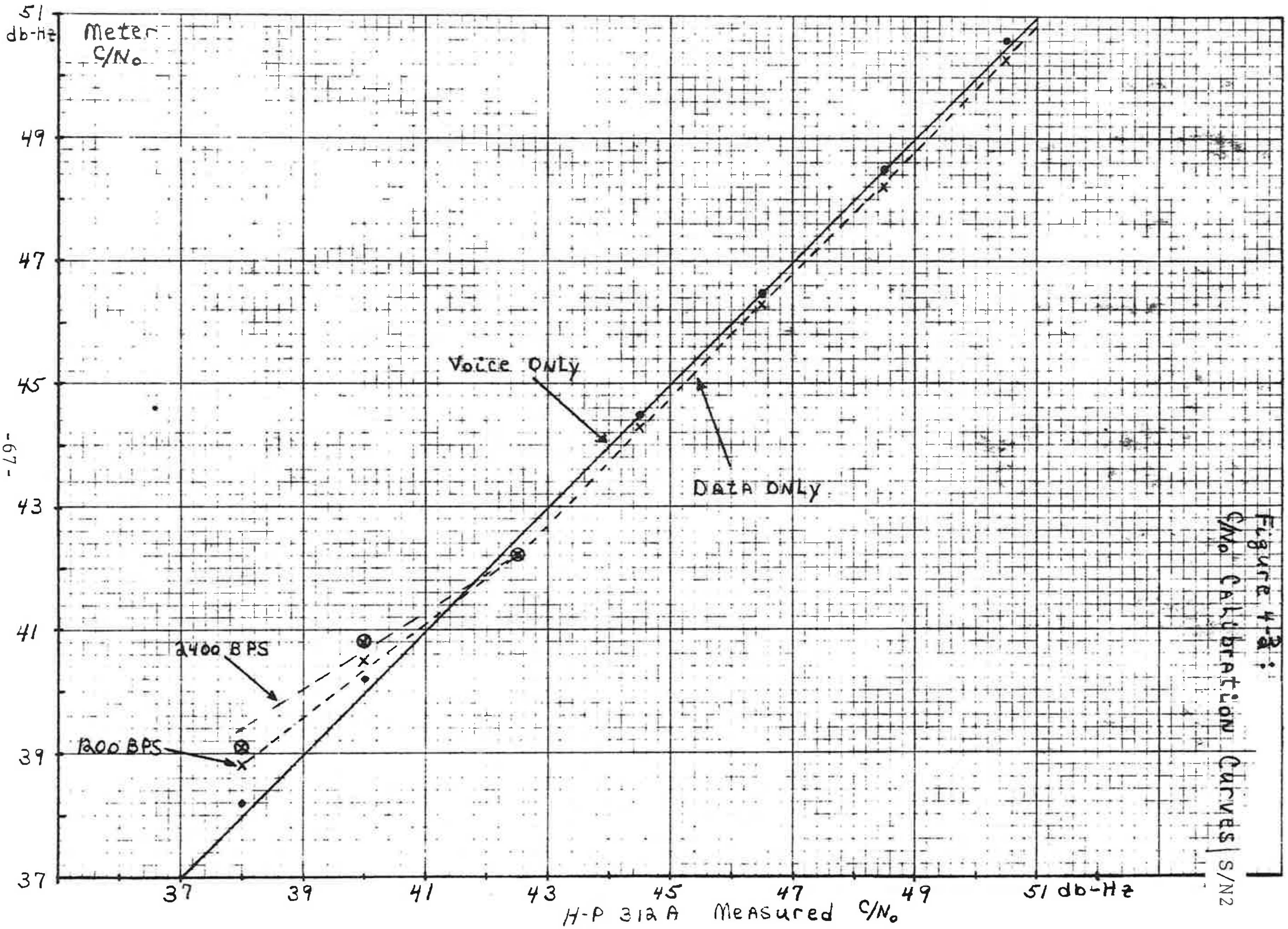


Figure 4-2:
C/No Calibration Curves
S/N2
Meter C/No
51 db-Hz
49
47
45
43
41
39
37
H-P 312A Measured C/No
37
39
41
43
45
47
49
51 db-Hz
Voice ONLY
DATA ONLY
2400 BPS
1200 BPS

FIGURE 4-4

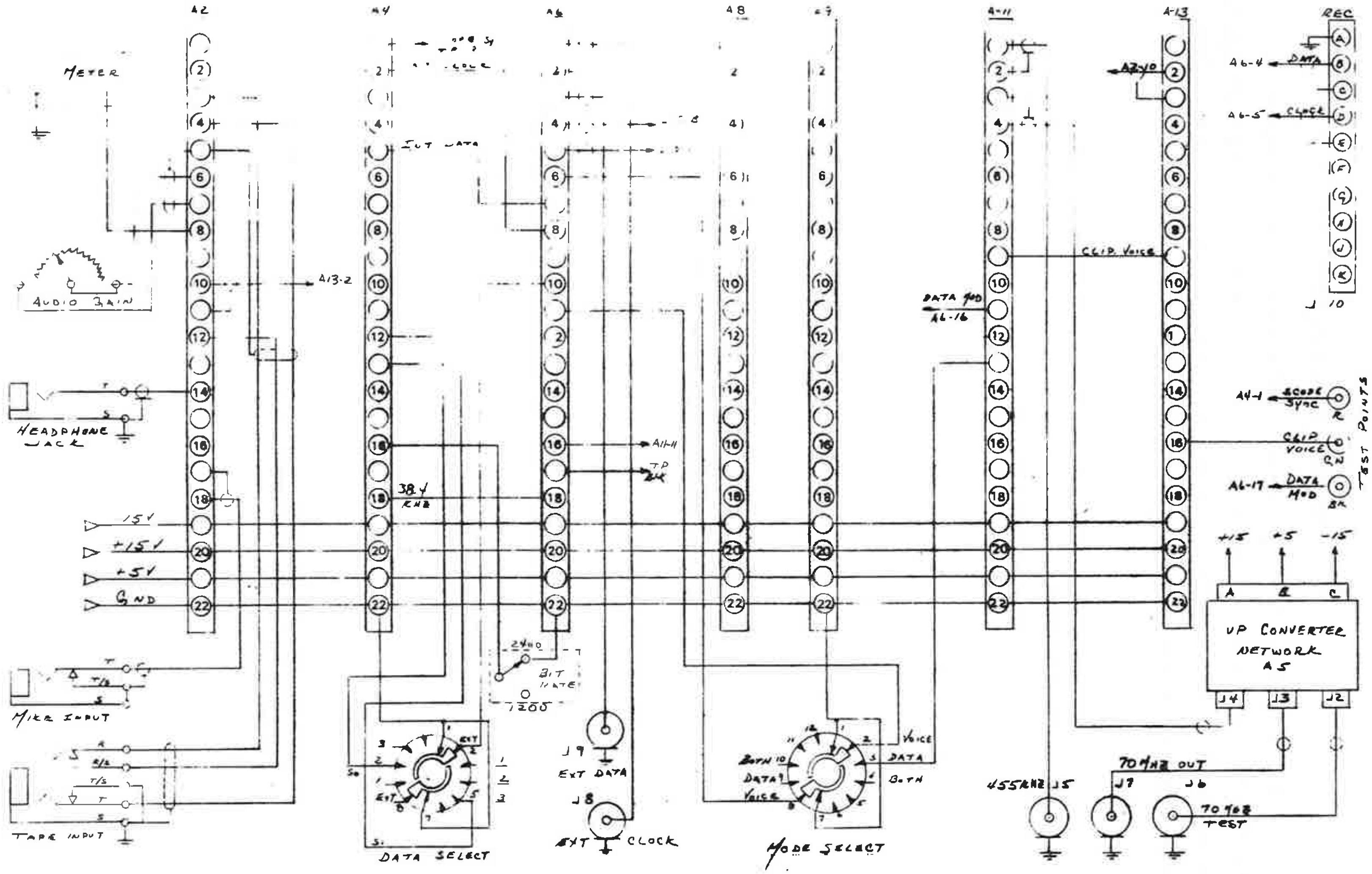
C/N_0 CALIBRATION DATA SHEET

ATTENUATOR SETTINGS		SELECTIVE VOLTMETER READINGS			C/N_o METER READING		
#1	#2	Signal	Noise	C/N_o	Voice	1200 BPS	2400 BPS

5. SCHEMATIC DIAGRAMS

A complete set of schematic diagrams for the Hybrid Modem Modulator and Demodulator is contained in this section. A schematic of each P.C. board is included along with wiring diagrams of both chassis.

F.gure … WIRING DIAGRAM



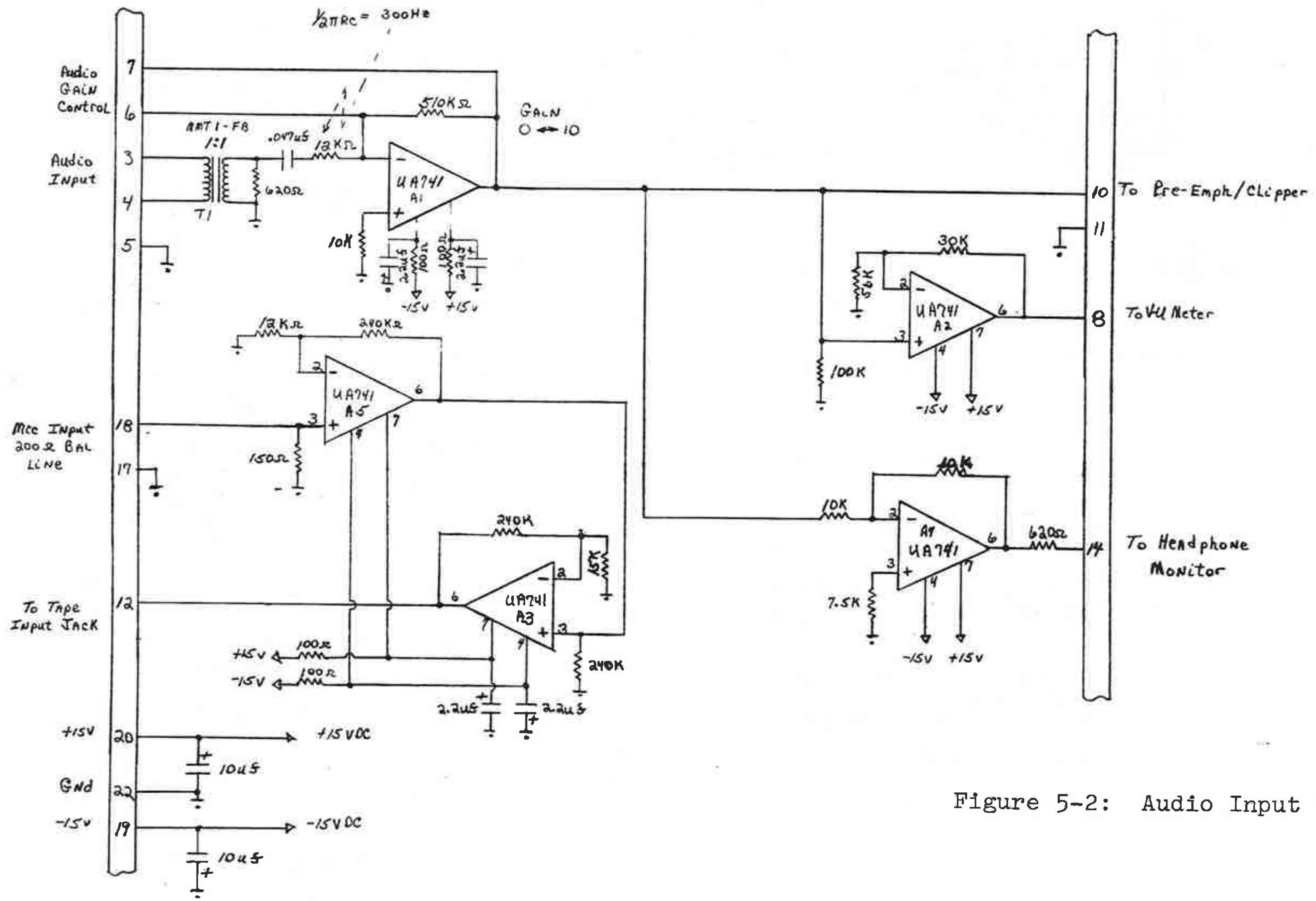
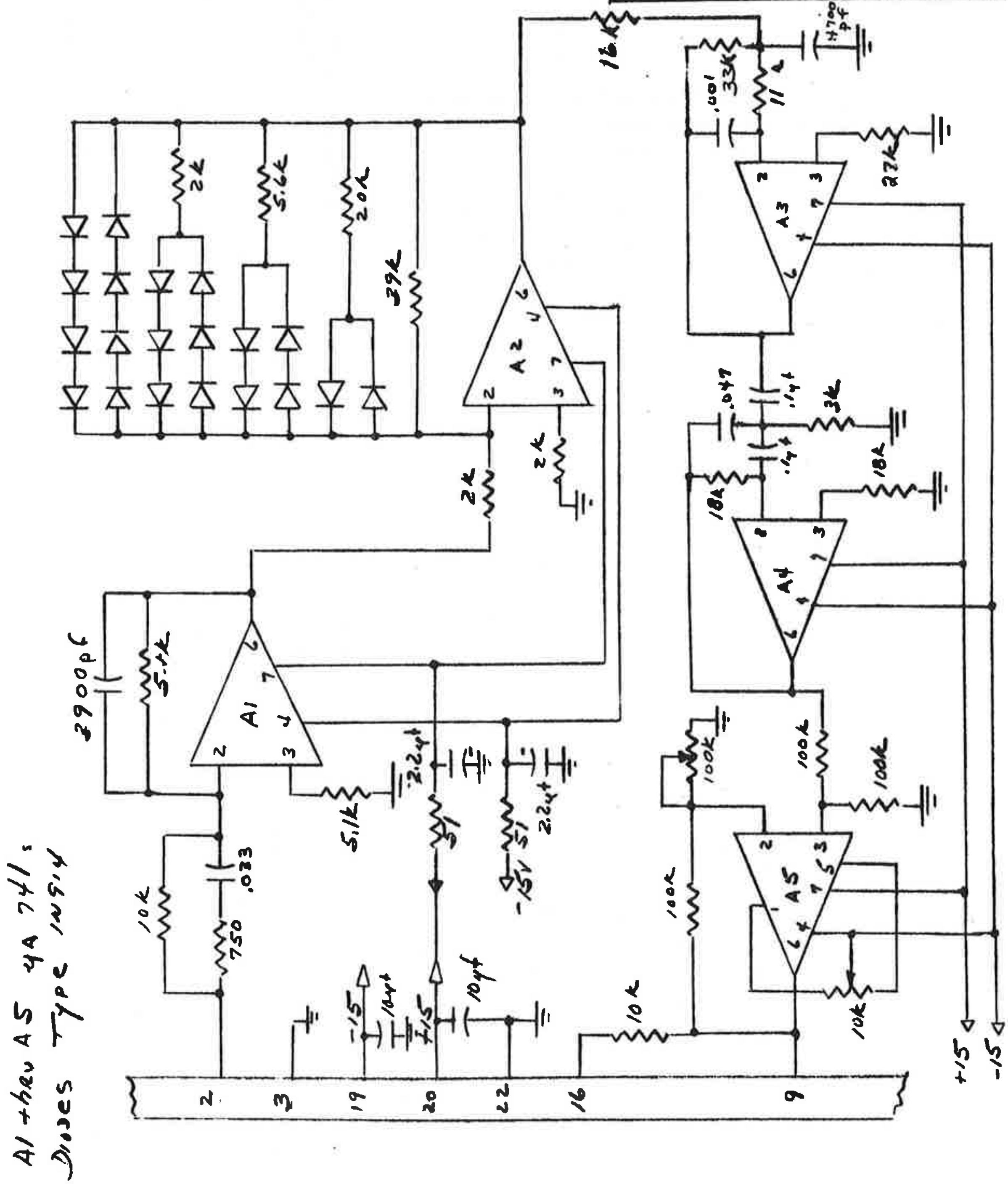


Figure 5-2: Audio Input Network

Figure 5-3: Voice Processing Network



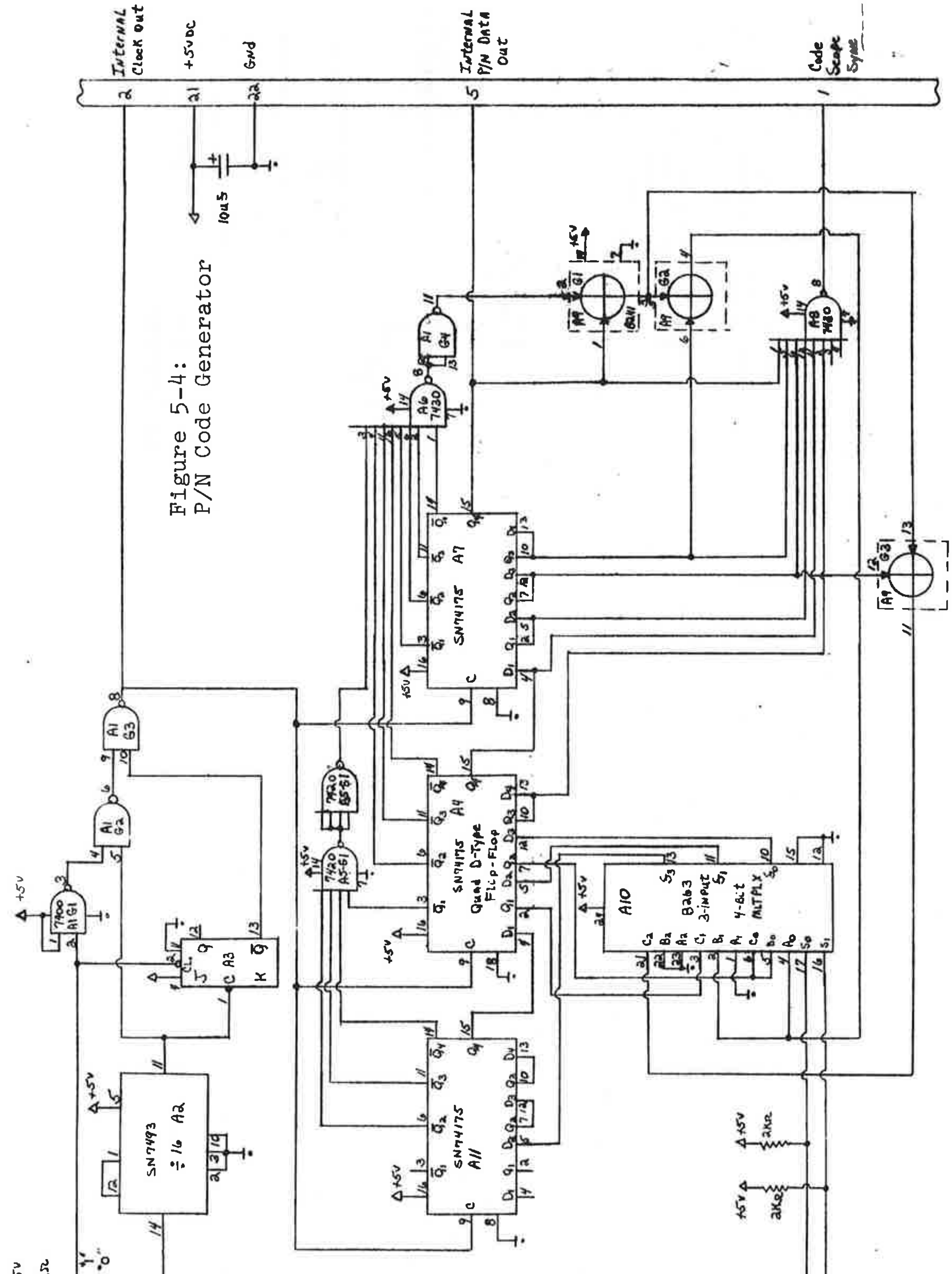


Figure 5-4:
P/N Code Generator

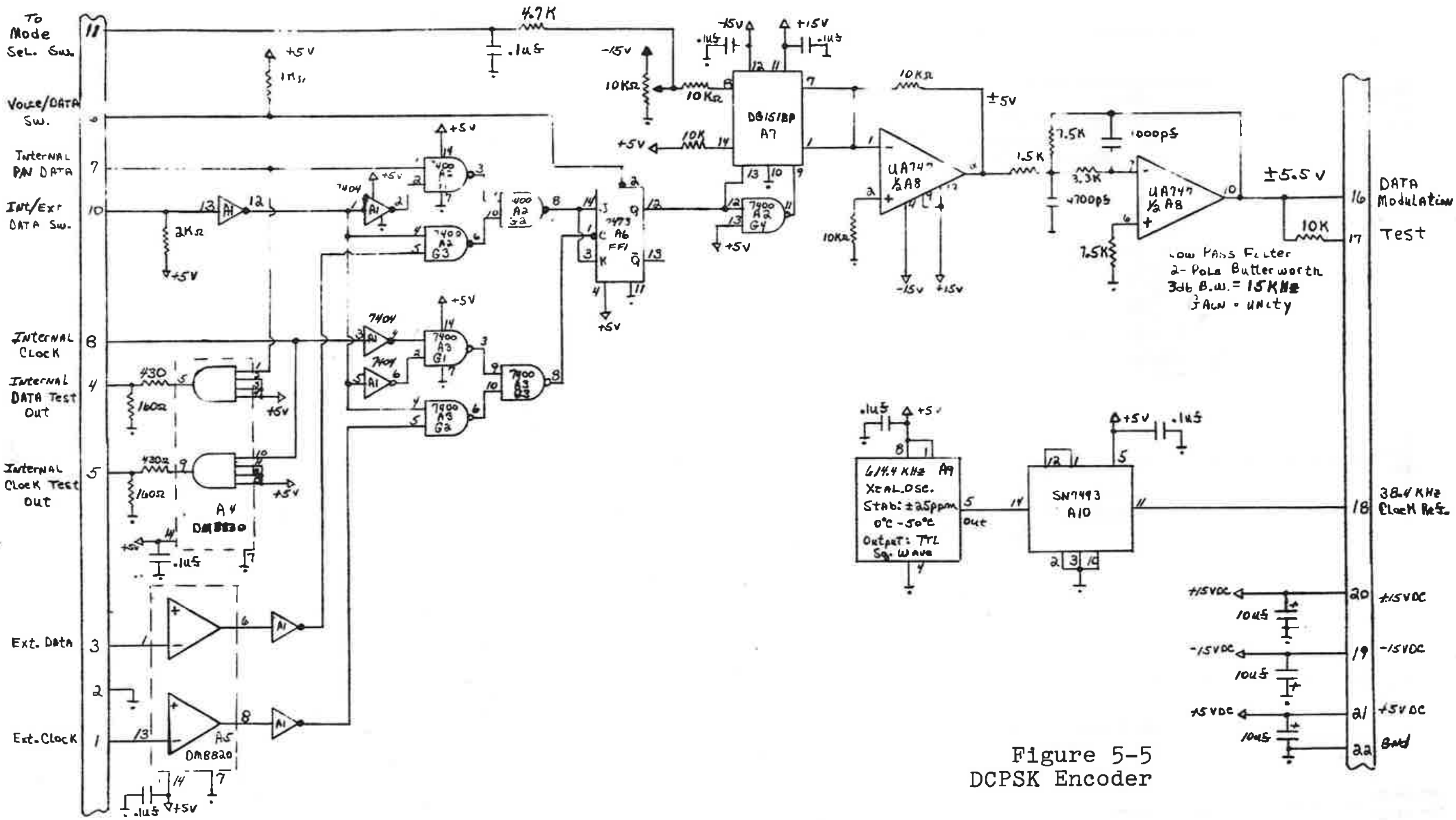


Figure 5-5
DCPSK Encoder

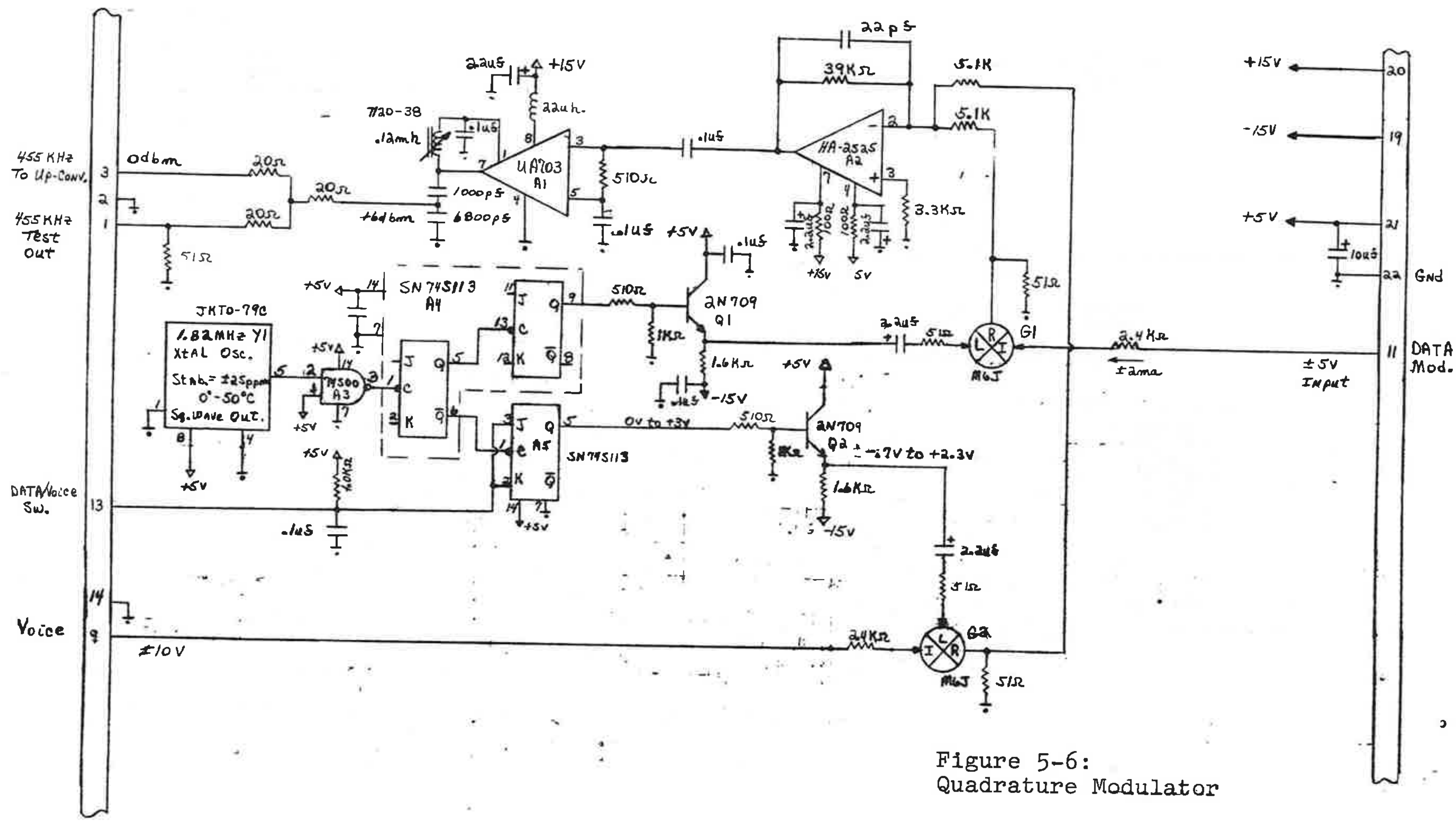


Figure 5-6:
Quadrature Modulator

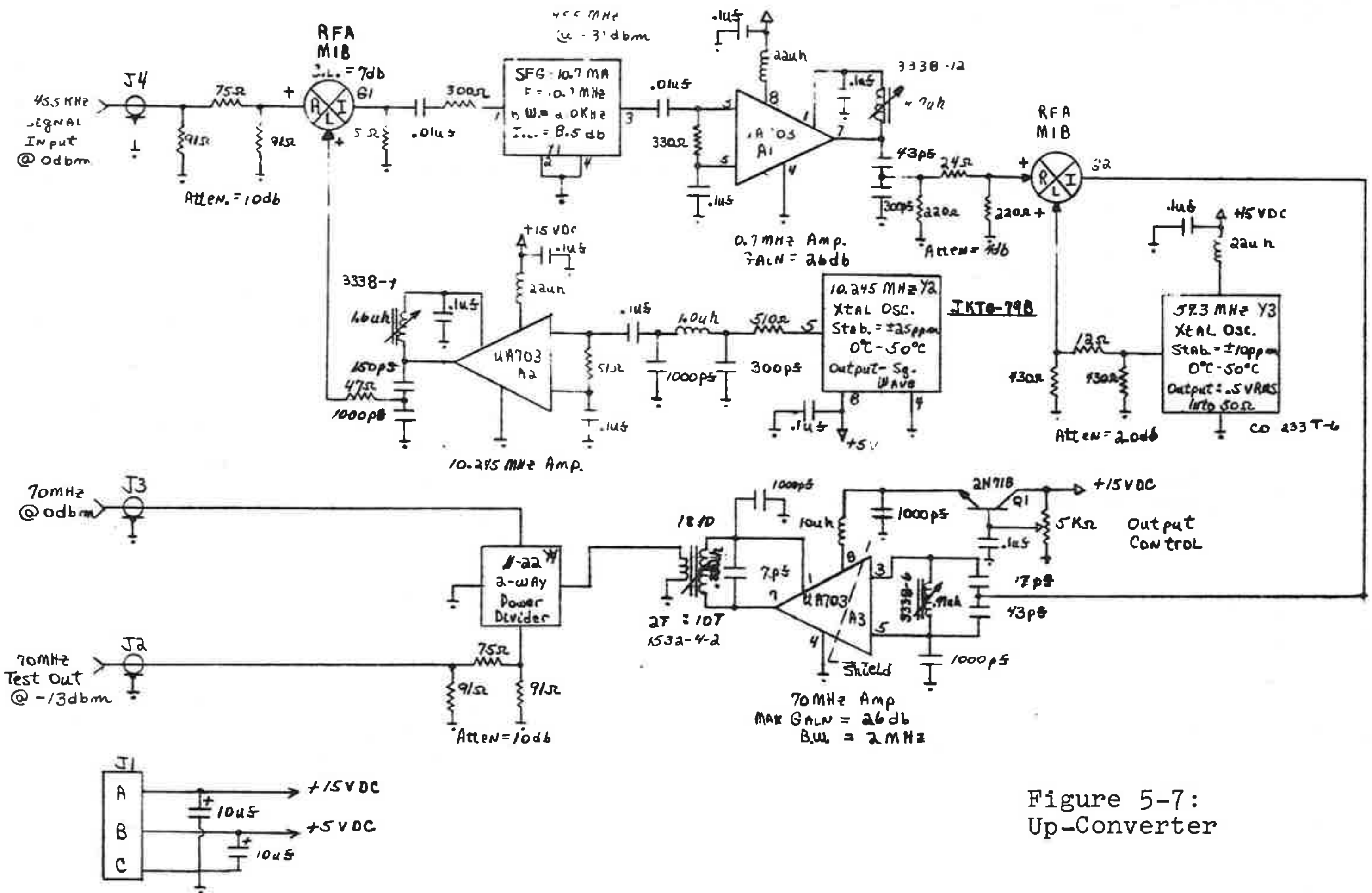
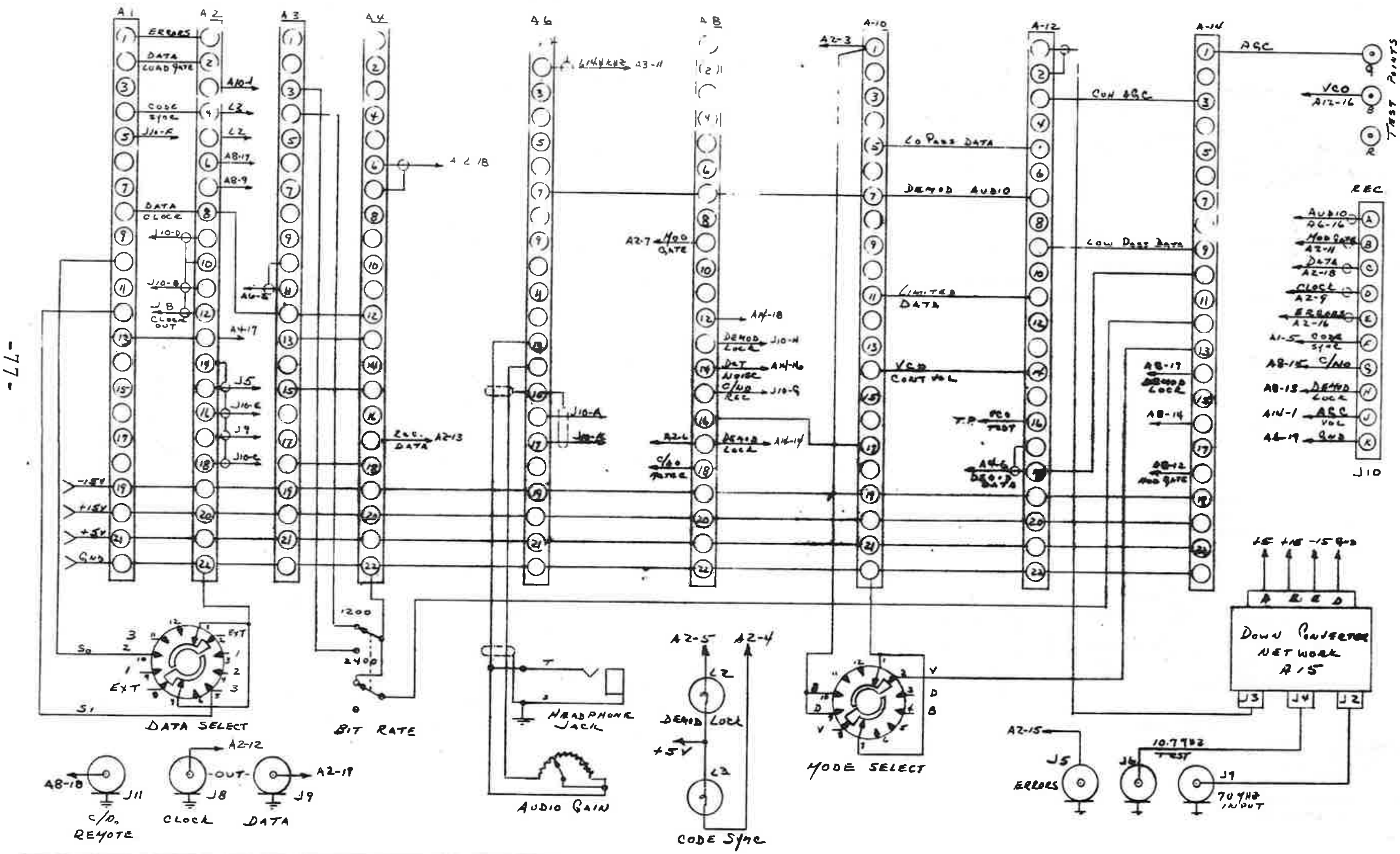


Figure 5-7:
Up-Converter

Figure 5.8: DEMODULATOR WIRING DIAGRAM



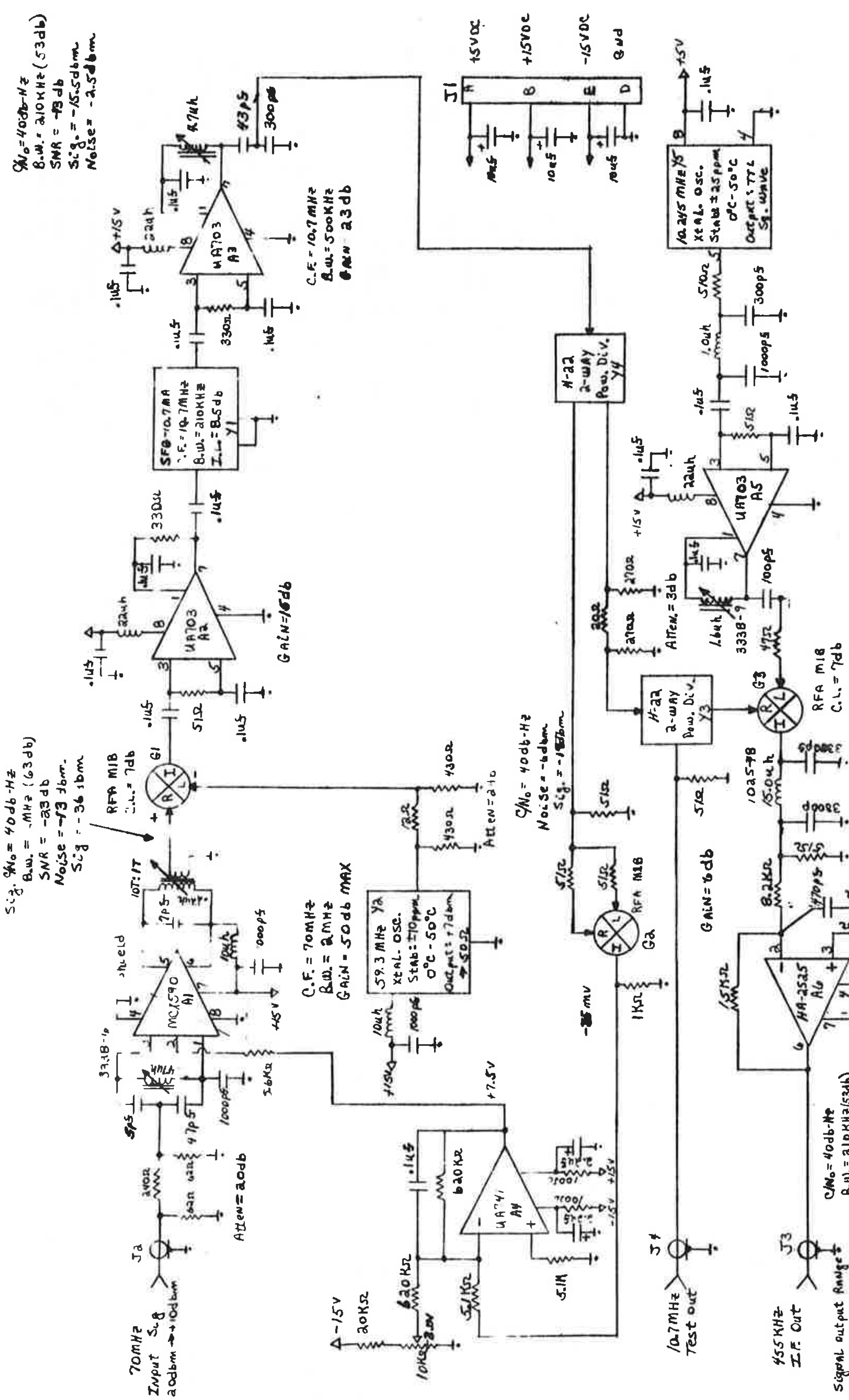


Figure 5-9:
Down-Converter

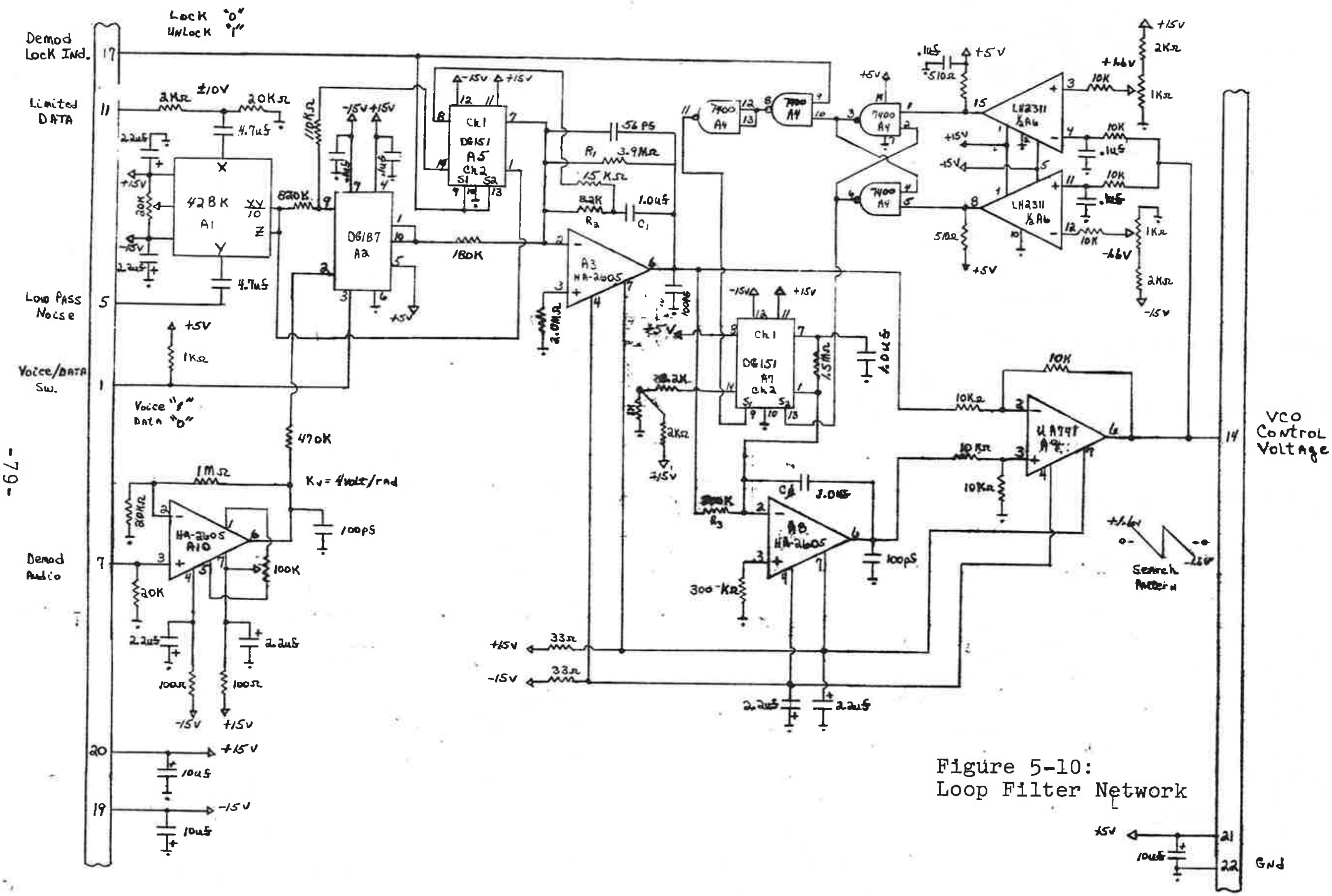


Figure 5-10:
Loop Filter Network

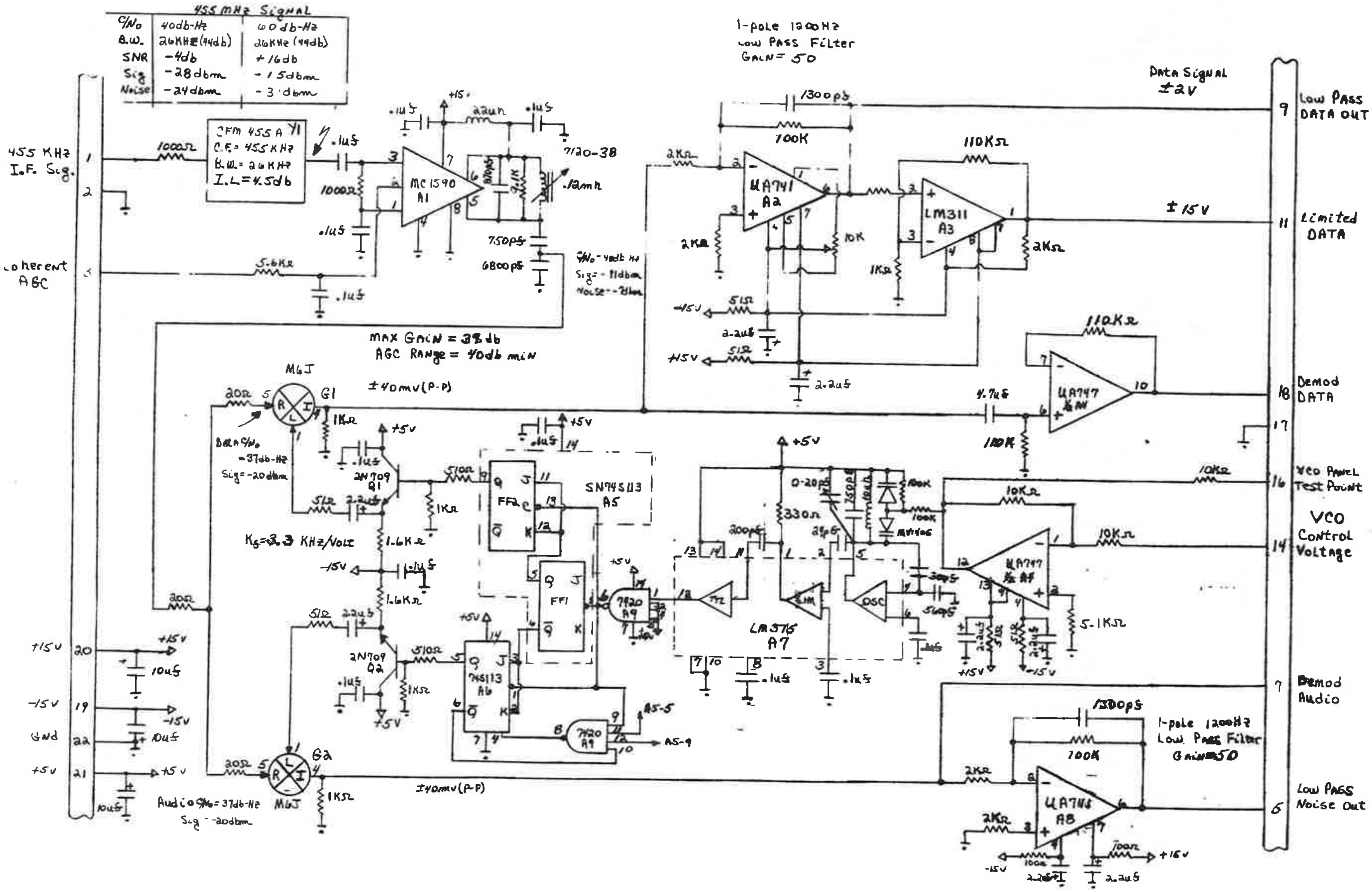


Figure 5-11:
455 kHz I.F. and AGC Network

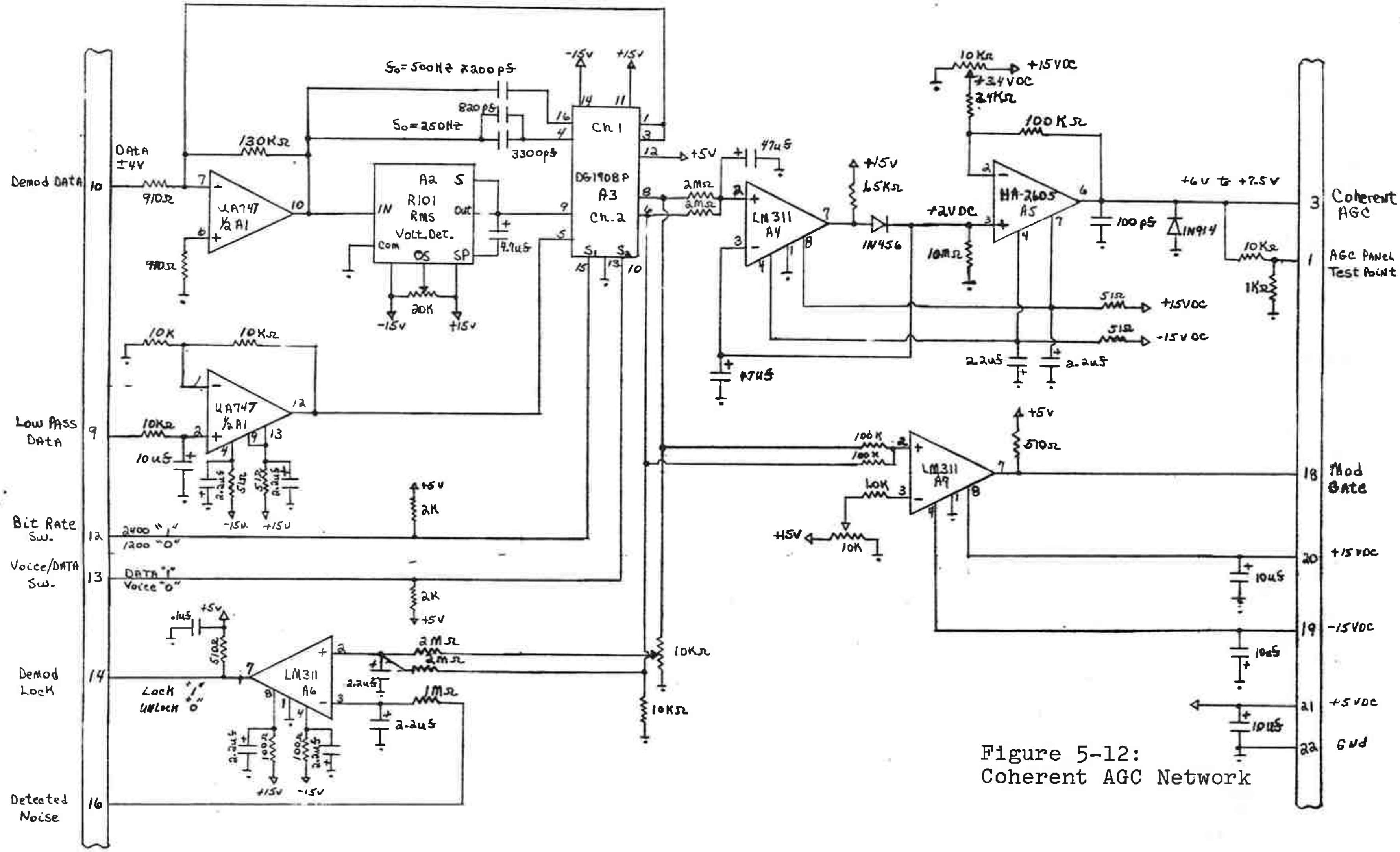
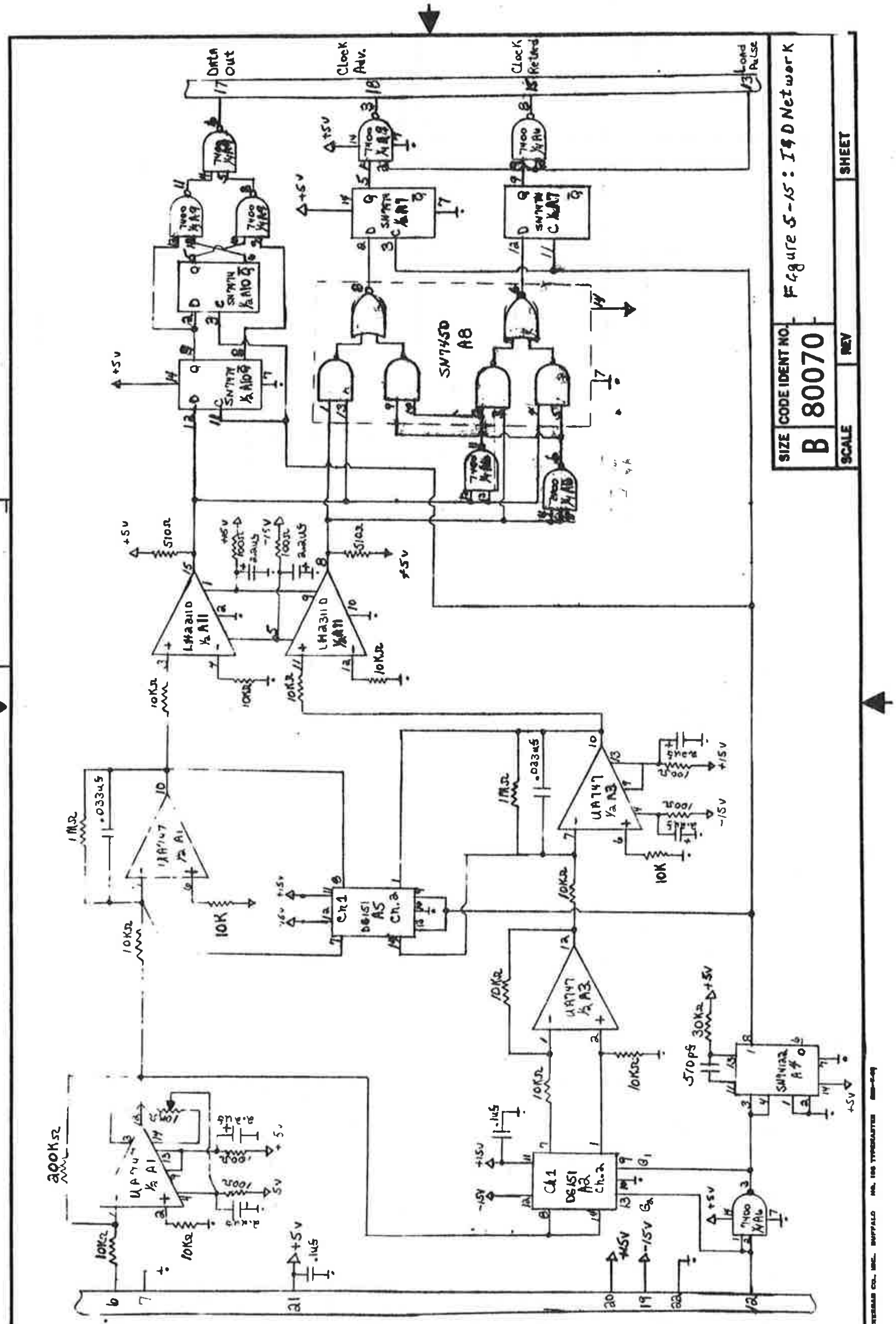
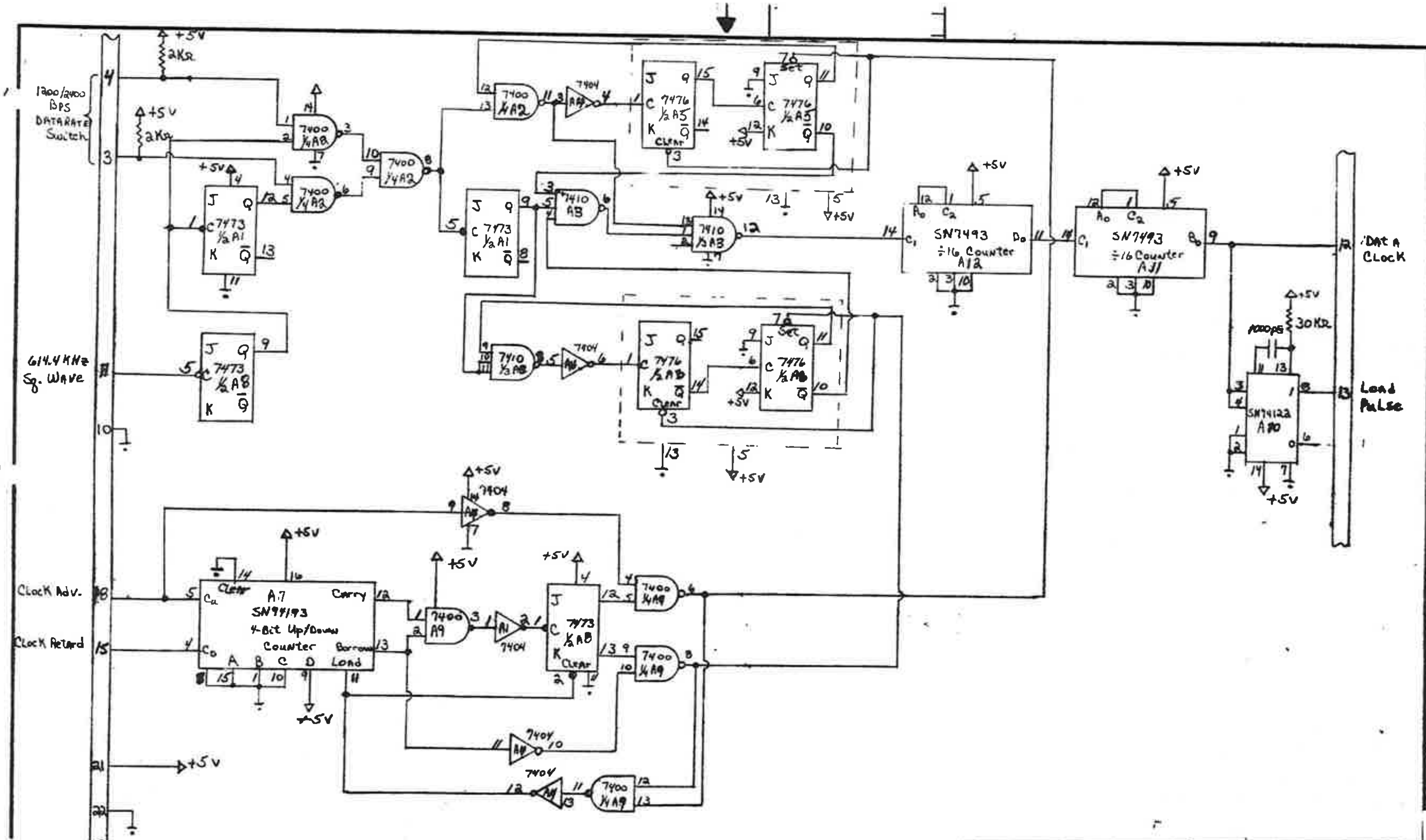


Figure 5-12:
Coherent AGC Network


Demod. DATA
DATA Clock
Data Out
Clock Adv.
Clock Retard
Load Pulse
SIZE
B
CODE IDENT NO.
80070
SCALE
REV
SHEET
Figure 5-15: I&D Network



SIZE	CODE IDENT NO.	
B	80070	Figure 5-16: Clock Sync Network
SCALE	REV	SHEET

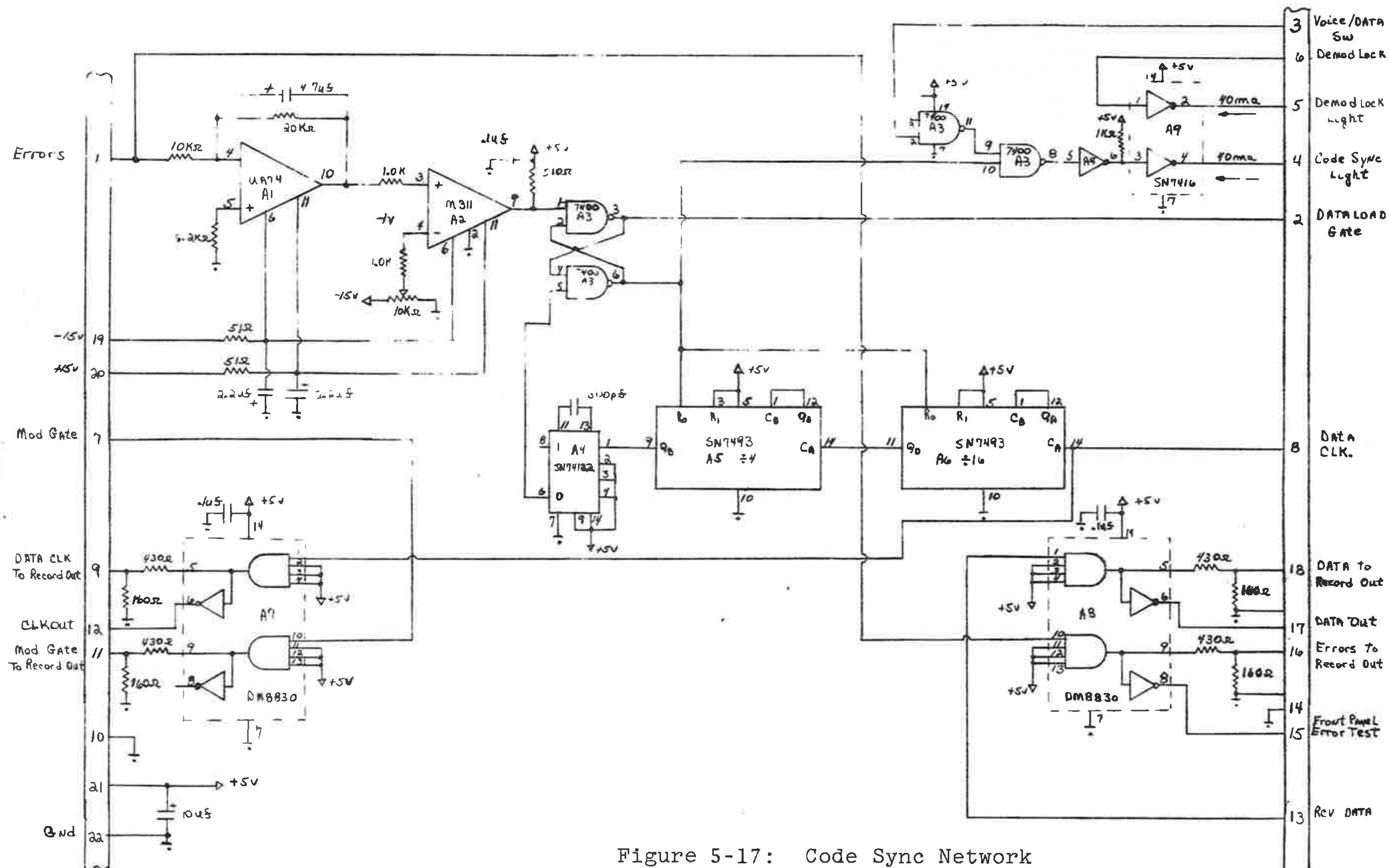


Figure 5-17: Code Sync Network

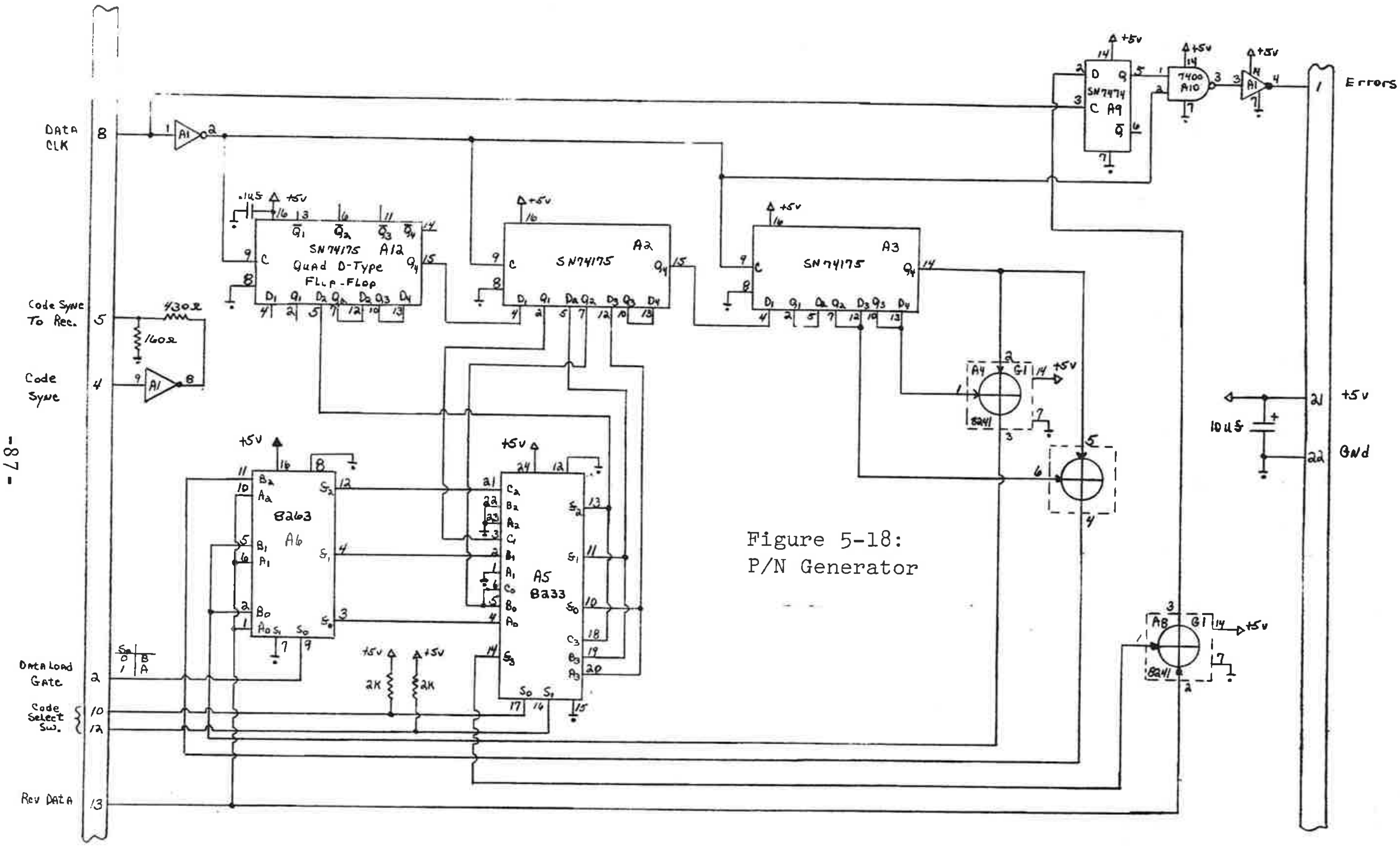


Figure 5-18:
P/N Generator

APPENDIX
REPORT OF INVENTIONS

After a diligent review of the work performed under this contract, no innovation, discovery, improvement, and/or invention was made.